



# THE DATASHEET OF NET+50-QIT-3

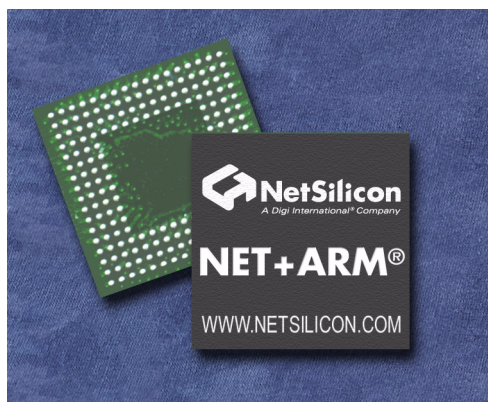




## *NET+50 Data Sheet*

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The Digi **NET+50** is a high-performance, highly integrated, 32-bit, system-on-a-chip ASIC, designed for use in intelligent networked devices and Internet appliances. The NET+50 is based on the standard architecture in the NET+ARM™ family of devices.



To support a variety of networking scenarios, the NET+50 includes a 10/100 BaseT Ethernet MAC with MII interface and two independent serial ports, each of which can run in UART, HDLC, or SPI mode.

The NET+50 CPU is an ARM7TDMI 32-bit RISC processor with a rich complement of support peripherals and memory controllers for various types of memory (including flash, SDRAM, EEPROM, and others), programmable timers, a 10-channel DMA controller, a P1284/ENI interface, an external bus expansion module, and up to 40 general-purpose I/O pins and 16 general-purpose input pins.

**NET+ARM** is the hardware foundation for the **NET+Works™** family of integrated hardware and software solutions for device networking. The NET+Works solution includes drivers, operating systems, networking software, development tools, APIs, and complete development boards.



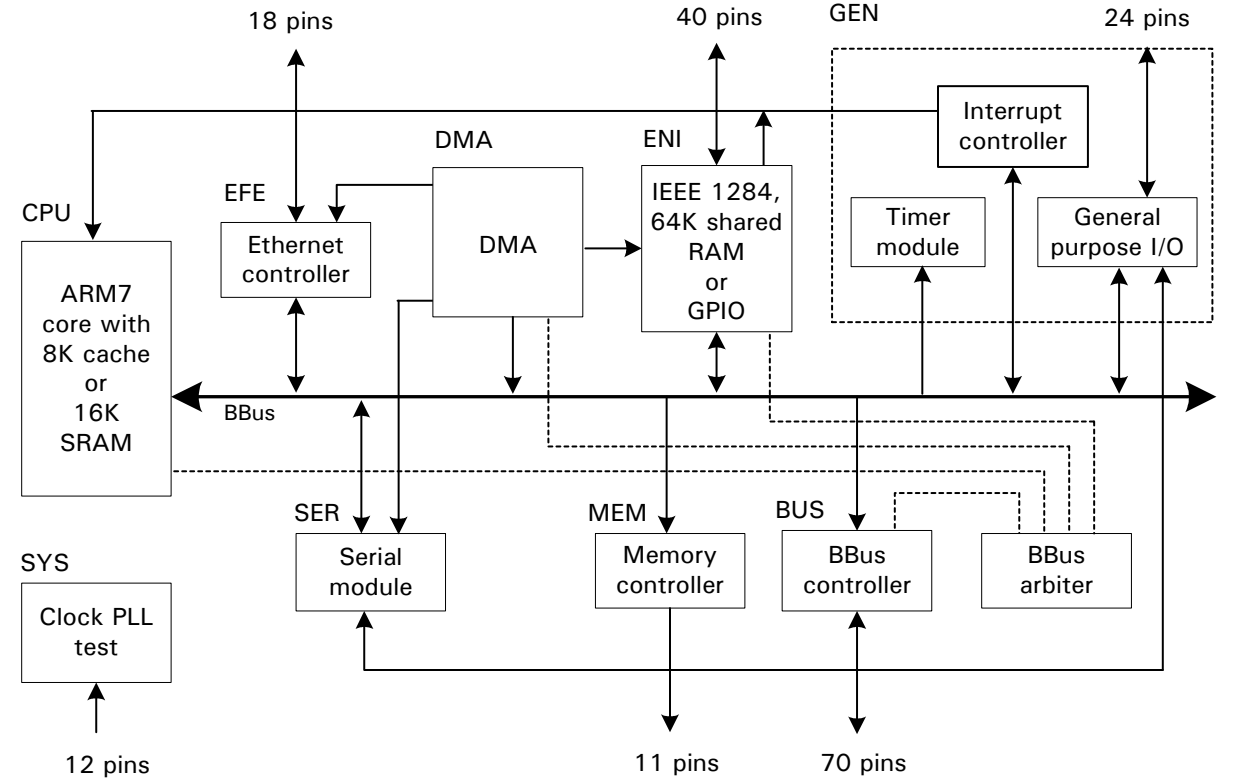
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## CPU core

- Full 32-bit ARM7TDMI RISC processor
- 32-bit internal bus
- 16-bit Thumb mode
- 8 KB cache, configurable as 16 KB RAM
- 15 general-purpose 32-bit registers
- 32-bit program counter and status register
- Five supervisor modes, one user mode

**Integrated 10/100 Ethernet MAC**

- 10/100 MII-based PHY interface
- 10 Mbit ENDEC interface
- Supports TP-PMD and fiber-PMD devices
- Full-duplex and half-duplex modes
- Optional 4B/5B coding
- Full statistics gathering (SNMP and RMON)
- Station, broadcast, and multicast address detection and filtering
- 128-byte transmit FIFO, 2 KB receive FIFO
- Intelligent receive-side buffer selection

**Operating frequency**

- 44-MHz maximum system clock, requiring only a simple external 18.432-MHz crystal
- Supports external oscillators

**ENI/P1284 Interface**

- ENI host interface
- Four IEEE 1284 parallel ports
- 64 KB shared RAM ENI interface — 8- or 16-bit
- Full-duplex FIFO mode interface — 8- or 16-bit
- 32-byte transmit/receive FIFO mode FIFOs

**Programmable timers**

- Two independent, 27-bit timers (2  $\mu$ s–20.7 hours)
- Watchdog timer (interrupt or reset on expiration)
- Bus timer

**Serial port**

- Two fully independent serial ports (UART, HDLC, SPI)
- Digital phase locked loop (DPLL) for receive clock extractions
- 32 byte transmit/receive FIFOs
- Internal programmable bit-rate generators
- Bit rates 75–230400 in 16X mode, 1200 bps – 4 Mbps in 1X mode. (Higher rates may be possible depending on the board design.)

**10-channel DMA controller**

- Two channels dedicated to Ethernet transmit and receive
- Four channels dedicated to serial transmit and receive
- Four channels (two at a time) configurable for external peripherals
- Flexible buffer management

**Bus interface**

- Five independent, programmable chip selects with 256 Mb addressing per chip select
- All chip selects support SRAM, EDO DRAM, SDRAM, and devices such as flash and EEPROM with SRAM interfaces
- Supports 8-, 16-, and 32-bit peripherals
- Dynamic bus sizing support
- Supports ASYNC and SYNC peripheral timing
- Internal DRAM address multiplexing
- Internal refresh controller (CAS before RAS)
- Burst-mode support
- 0–15 wait states per chip select
- Bootstrap support

**Power and operating voltages**

- 552 mW maximum (typically, 484 mW), outputs switching
- 3.3 V — I/O
- 2.5 V — core

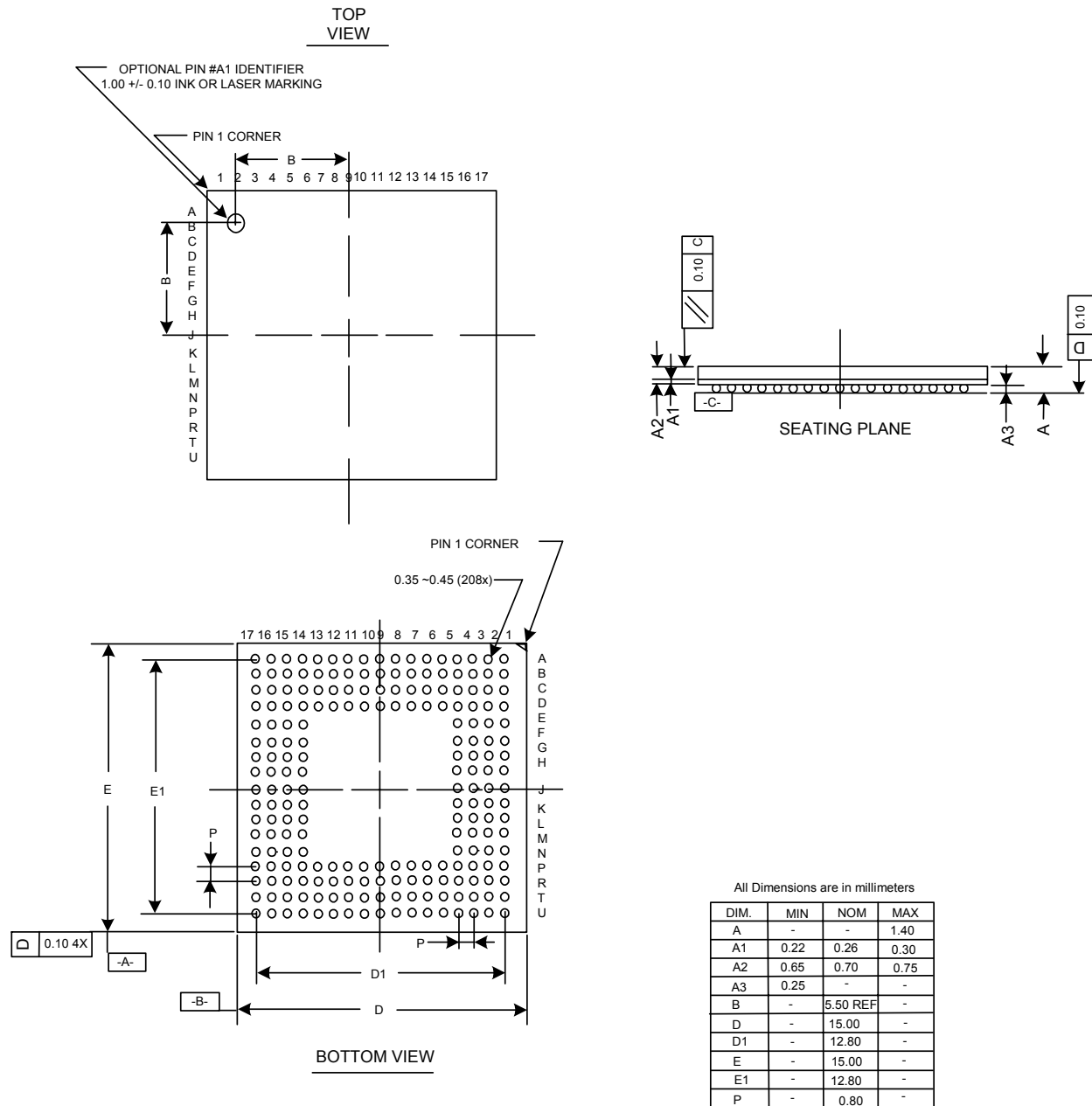
**Serial port (cont)**

- Odd, even, or no parity
- 5, 6, 7, or 8 bits
- 1 or 2 stop bits
- Internal and external clock support
- Receive-side character and buffer gap timers
- Four receive-side data match detectors

## Packaging dimensions and pinout

The NET+50 is available in two package options – a ball-grid array (BGA) or a plastic quad flat pack (PQFP).

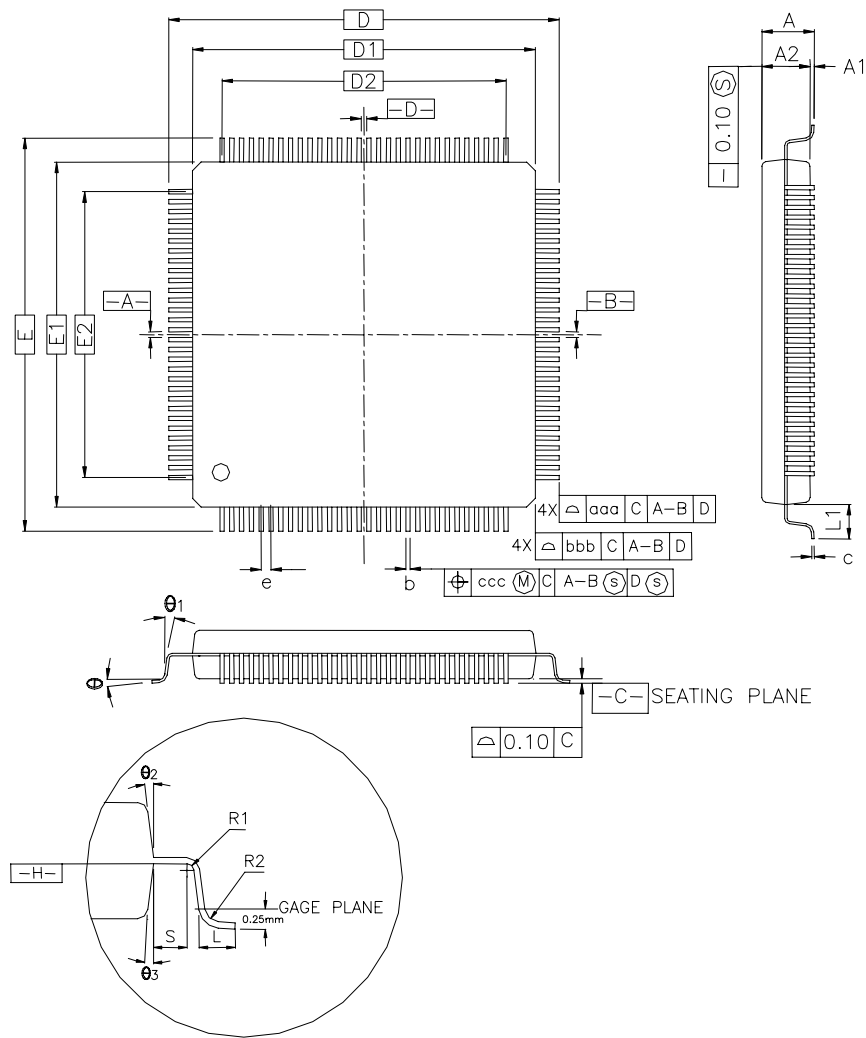
### BGA packaging and pinout diagram





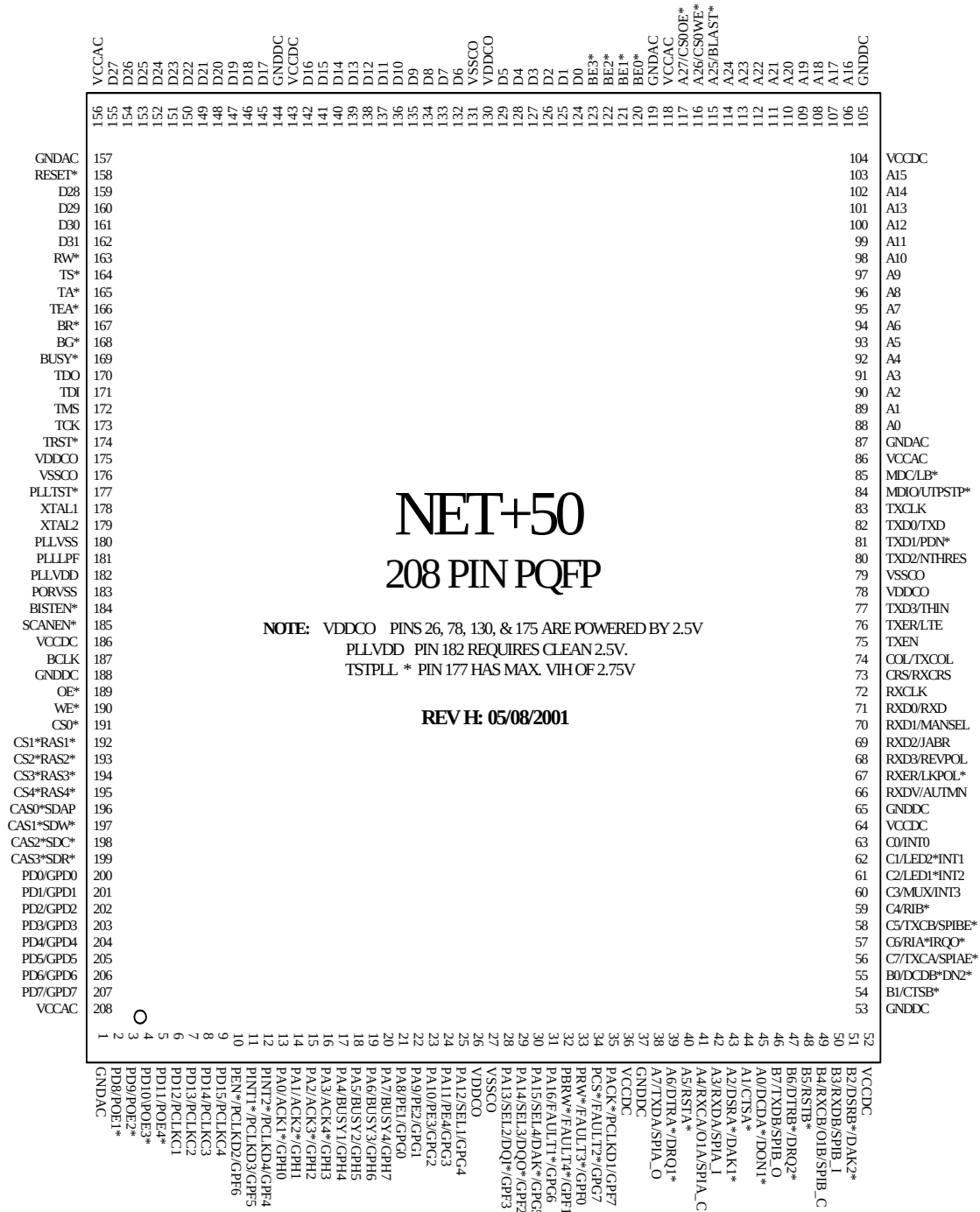
PQFP packaging and pinout diagrams

PQFP packaging



COTROL DIMENSIONS ARE IN MILLIMETERS.

| SYMBOL                          | MILLIMETER  |      |      | INCH        |       |       |
|---------------------------------|-------------|------|------|-------------|-------|-------|
|                                 | MIN.        | NOM. | MAX. | MIN.        | NOM.  | MAX.  |
| A                               | —           | —    | 4.10 | —           | —     | 0.161 |
| A1                              | 0.25        | —    | —    | 0.010       | —     | —     |
| A2                              | 3.20        | 3.32 | 3.60 | 0.126       | 0.131 | 0.142 |
| D                               | 31.20 BASIC |      |      | 1.228 BASIC |       |       |
| D1                              | 28.00 BASIC |      |      | 1.102 BASIC |       |       |
| E                               | 31.20 BASIC |      |      | 1.228 BASIC |       |       |
| E1                              | 28.00 BASIC |      |      | 1.102 BASIC |       |       |
| R2                              | 0.13        | —    | 0.30 | 0.005       | —     | 0.012 |
| R1                              | 0.13        | —    | —    | 0.005       | —     | —     |
| θ                               | 0°          | —    | 7°   | 0°          | —     | 7°    |
| θ1                              | 0°          | —    | —    | 0°          | —     | —     |
| θ2                              | 8° REF      |      |      | 8° REF      |       |       |
| θ3                              | 8° REF      |      |      | 8° REF      |       |       |
| c                               | 0.11        | 0.15 | 0.23 | 0.004       | 0.006 | 0.009 |
| L                               | 0.73        | 0.88 | 1.03 | 0.029       | 0.035 | 0.041 |
| L1                              | 1.60 REF    |      |      | 0.063 REF   |       |       |
| S                               | 0.20        | —    | —    | 0.008       | —     | —     |
| b                               | 0.17        | 0.20 | 0.27 | 0.007       | 0.008 | 0.011 |
| e                               | 0.50 BSC.   |      |      | 0.020 BSC.  |       |       |
| D2                              | 25.50       |      |      | 1.004       |       |       |
| E2                              | 25.50       |      |      | 1.004       |       |       |
| TOLERANCES OF FORM AND POSITION |             |      |      |             |       |       |
| aaa                             | 0.25        |      |      | 0.010       |       |       |
| bbb                             | 0.20        |      |      | 0.008       |       |       |
| ccc                             | 0.08        |      |      | 0.003       |       |       |

**PQFP pinout**

## Pinout detail tables

The pinout tables in the following sections have the following columns:

|        |                                                                                                                                                                                                                                               |
|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Signal | The pin name for each I/O signal. Some signals have dual modes and are identified accordingly. The mode is configured through firmware using a configuration register. Some modes may require hardware configuration during a RESET condition |
| BGA    | The BGA pin number for specific I/O signals.                                                                                                                                                                                                  |
| PQFP   | The PQFP pin number for specific I/O signals.                                                                                                                                                                                                 |
| †      | A dagger indicates a pin that is an input current source. (The daggers appear in the BGA column, but this applies in PQFP layout as well.)                                                                                                    |
| *      | An asterisk indicates a pin that is <i>active low</i> .                                                                                                                                                                                       |
| I/O    | The type of signal — input, output, or input/output (I/O).                                                                                                                                                                                    |
| OD     | The output drive strength of an output buffer. The NET + 50 uses one of three drivers: <ul style="list-style-type: none"> <li>■ 2 mA</li> <li>■ 4 mA</li> <li>■ 8 mA</li> </ul>                                                               |

## System bus interface

| Signal |        | BGA  | PQFP | I/O | OD | Description           |                             |
|--------|--------|------|------|-----|----|-----------------------|-----------------------------|
| BCLK   |        | T10  | 187  | O   | 8  | Synchronous bus clock |                             |
| ADDR27 | CS0OE* | F4 † | 117  | I/O | 4  | Address bus           | Chip select 0 output enable |
| ADDR26 | CS0WE* | F3 † | 116  | I/O | 4  | Address bus           | Chip select 0 write enable  |
| ADDR25 | BLAST* | E2 † | 115  | I/O | 4  | Address bus           | Burst-terminated input      |
| ADDR24 |        | D2 † | 114  | I/O | 4  |                       |                             |
| ADDR23 |        | E3 † | 113  | I/O | 4  |                       |                             |
| ADDR22 |        | E4 † | 112  | I/O | 4  |                       |                             |
| ADDR21 |        | D1 † | 111  | I/O | 4  |                       |                             |
| ADDR20 |        | C2 † | 110  | I/O | 4  |                       |                             |
| ADDR19 |        | D3 † | 109  | I/O | 4  |                       |                             |
| ADDR18 |        | C1 † | 108  | I/O | 4  |                       |                             |
| ADDR17 |        | B1 † | 107  | I/O | 4  |                       |                             |
| ADDR16 |        | B2 † | 106  | I/O | 4  |                       |                             |
| ADDR15 |        | B3 † | 103  | I/O | 4  |                       |                             |
| ADDR14 |        | A3 † | 102  | I/O | 4  |                       |                             |
| ADDR13 |        | A4 † | 101  | I/O | 4  |                       |                             |
| ADDR12 |        | B4 † | 100  | I/O | 4  |                       |                             |

**System bus interface (cont.)**

| Signal | BGA  | PQFP | I/O | OD | Description |
|--------|------|------|-----|----|-------------|
| ADDR11 | C3 † | 99   | I/O | 4  |             |
| ADDR10 | A5 † | 98   | I/O | 4  |             |
| ADDR9  | D4 † | 97   | I/O | 4  |             |
| ADDR8  | C4 † | 96   | I/O | 4  |             |
| ADDR7  | B5 † | 95   | I/O | 4  |             |
| ADDR6  | A6 † | 94   | I/O | 4  |             |
| ADDR5  | D5 † | 93   | I/O | 4  |             |
| ADDR4  | C5 † | 92   | I/O | 4  |             |
| ADDR3  | B6 † | 91   | I/O | 4  |             |
| ADDR2  | A7 † | 90   | I/O | 4  |             |
| ADDR1  | D6 † | 89   | I/O | 4  |             |
| ADDR0  | C6 † | 88   | I/O | 4  |             |
| DATA31 | T3   | 162  | I/O | 4  | Data bus    |
| DATA30 | R4   | 161  | I/O | 4  |             |
| DATA29 | U3   | 160  | I/O | 4  |             |
| DATA28 | U2   | 159  | I/O | 4  |             |
| DATA27 | R2   | 155  | I/O | 4  |             |
| DATA26 | R1   | 154  | I/O | 4  |             |
| DATA25 | P1   | 153  | I/O | 4  |             |
| DATA24 | P2   | 152  | I/O | 4  |             |
| DATA23 | R3   | 151  | I/O | 4  |             |
| DATA22 | N1   | 150  | I/O | 4  |             |
| DATA21 | P4   | 149  | I/O | 4  |             |
| DATA20 | P3   | 148  | I/O | 4  |             |
| DATA19 | N2   | 147  | I/O | 4  |             |
| DATA18 | M1   | 146  | I/O | 4  |             |
| DATA17 | N4   | 145  | I/O | 4  |             |
| DATA16 | L1   | 142  | I/O | 4  |             |
| DATA15 | M4   | 141  | I/O | 4  |             |
| DATA14 | M3   | 140  | I/O | 4  |             |
| DATA13 | L2   | 139  | I/O | 4  |             |
| DATA12 | K1   | 138  | I/O | 4  |             |

## System bus interface (cont.)

| Signal | BGA        | PQFP | I/O | OD | Description                     |
|--------|------------|------|-----|----|---------------------------------|
| DATA11 | L4         | 137  | I/O | 4  |                                 |
| DATA10 | L3         | 136  | I/O | 4  |                                 |
| DATA9  | K2         | 135  | I/O | 4  |                                 |
| DATA8  | J1         | 134  | I/O | 4  |                                 |
| DATA7  | K4         | 133  | I/O | 4  |                                 |
| DATA6  | K3         | 132  | I/O | 4  |                                 |
| DATA5  | J4         | 129  | I/O | 4  |                                 |
| DATA4  | J3         | 128  | I/O | 4  |                                 |
| DATA3  | H2         | 127  | I/O | 4  |                                 |
| DATA2  | G1         | 126  | I/O | 4  |                                 |
| DATA1  | H4         | 125  | I/O | 4  |                                 |
| DATA0  | H3         | 124  | I/O | 4  |                                 |
| TS*    | no connect |      |     |    |                                 |
| BE3*   | G2         | 123  | I/O | 2  | Byte enable D31:D24             |
| BE2*   | F1         | 122  | I/O | 2  | Byte enable D23:D16             |
| BE1*   | G4         | 121  | I/O | 2  | Byte enable D15:D08             |
| BE0*   | G3         | 120  | I/O | 2  | Byte enable D07:D00             |
| RW*    | U4         | 163  | I/O | 2  | Transfer direction              |
| TA*    | R5 †       | 165  | I/O | 8  | Data transfer acknowledge       |
| TEA*   | T4 †       | 166  | I/O | 8  | Transfer error/last acknowledge |
| BR*    | no connect |      |     |    |                                 |
| BG*    | no connect |      |     |    |                                 |
| BUSY*  | no connect |      |     |    |                                 |

## Chip select controller

| Signal |         | BGA | PQFP | I/O | OD | Description               |             |
|--------|---------|-----|------|-----|----|---------------------------|-------------|
| CS0 *  |         | T11 | 191  | O   | 4  | Chip select (boot select) |             |
| CS1 *  | RAS1 *  | R12 | 192  | O   | 4  | Chip select               | DRAM RAS *  |
| CS2 *  | RAS2 *  | P12 | 193  | O   | 4  | Chip select               | DRAM RAS *  |
| CS3 *  | RAS3 *  | U11 | 194  | O   | 4  | Chip select               | DRAM RAS *  |
| CS4 *  | RAS4 *  | T12 | 195  | O   | 4  | Chip select               | DRAM RAS *  |
| CAS3 * | SDRAS * | T13 | 199  | O   | 4  | DRAM column strobe D31:24 | SDRAM RAS * |
| CAS2 * | SDCAS * | U12 | 198  | O   | 4  | DRAM column strobe D23:16 | SDRAM CAS * |
| CAS1 * | SDWE *  | P13 | 197  | O   | 4  | DRAM column strobe D15:08 | SDRAM WE *  |
| CAS0 * | SD(AP)  | R13 | 196  | O   | 4  | DRAM column strobe D07:00 | SDRAM (AP)  |
| WE *   |         | R11 | 190  | O   | 4  | Write enable              |             |
| OE *   |         | P11 | 189  | O   | 4  | Output enable             |             |

## Ethernet interface

| MII   | 10BaseT    | BGA  | PQFP | I/O | OD | MII           | 10BaseT              |
|-------|------------|------|------|-----|----|---------------|----------------------|
| MDC   | LB *       | D7   | 85   | O   | 2  | MII clock     | Loopback enable      |
| MDIO  | UTPSTP *   | C7 † | 84   | I/O | 2  | MII data      | Cable type           |
| TXCLK | TXCLK      | B8   | 83   | I   |    | TX clock      |                      |
| TXD0  | TXD        | A9   | 82   | O   | 2  | TX data 0     | TX data              |
| TXD1  | PDN * (OD) | D8   | 81   | O   | 2  | TX data 1     | Power down           |
| TXD2  | NTHRES     | C8   | 80   | O   | 2  | TX data 2     | Normal threshold     |
| TXD3  | THIN       | D9   | 77   | O   | 2  | TX data 3     | Enable Thinnet       |
| TXER  | LTE        | C9   | 76   | O   | 2  | TX code error | Link test enable     |
| TXEN  | TXEN       | B10  | 75   | O   | 2  | TX enable     |                      |
| COL   | TXCOL      | A11  | 74   | I   |    | Collision     |                      |
| CRS   | RXCRC      | D10  | 73   | I   |    | Carrier sense |                      |
| RXCLK | RXCLK      | C10  | 72   | I   |    | RX clock      |                      |
| RXD0  | RXD        | B11  | 71   | I   |    | RX data 0     | RX data              |
| RXD1  | MANSENSE   | A12  | 70   | I   |    | RX data 1     | Sense jumper         |
| RXD2  | JABBER     | D11  | 69   | I   |    | RX data 2     | Jabber               |
| RXD3  | REVPOL     | C11  | 68   | I   |    | RX data 3     | Reverse polarity     |
| RXER  | LINKPUL *  | B12  | 67   | I   |    | RX error      | Link pulse detection |
| RXDV  | AUTOMAN    | A13  | 66   | I   |    | RX data valid | 10B2 selected        |

## UARTs, SPI, and GPIO

| GPIO   | UART /<br>HDLC | Special /<br>DMA mode | BGA   | PQFP | I/O | OD | SPI<br>slave mode             | SPI<br>master mode |
|--------|----------------|-----------------------|-------|------|-----|----|-------------------------------|--------------------|
| PORTA7 | TXDA           |                       | G17 † | 38   | I/O | 2  | SPI-S-TXD-O-A                 | SPI-M-TXD-O-A      |
| PORTA6 | DTRA*          | DRQ1*                 | F16 † | 39   | I/O | 2  |                               |                    |
| PORTA5 | RTSA*          |                       | E15 † | 40   | I/O | 2  |                               |                    |
| PORTA4 |                | RXCA                  | E14 † | 41   | I/O | 2  | SPI-S-CLK-I-A                 | SPI-M-CLK-O-A      |
| PORTA3 | RXDA           |                       | F17 † | 42   | I/O | 2  | SPI-S-RXD-I-A                 | SPI-M-RXD-I-A      |
| PORTA2 | DSRA*          | DAK1*                 | E16 † | 43   | I/O | 2  |                               |                    |
| PORTA1 | CTSA*          |                       | D15 † | 44   | I/O | 2  |                               |                    |
| PORTA0 | DCDA*          | DON1*                 | D14 † | 45   | I/O | 2  |                               |                    |
| PORTB7 | TXDB           |                       | E17 † | 46   | I/O | 2  | SPI-S-TXD-O-B                 | SPI-M-TXD-O-B      |
| PORTB6 | DTRB*          | DRQ2*                 | C15 † | 47   | I/O | 2  |                               |                    |
| PORTB5 | RTSB*          |                       | D16 † | 48   | I/O | 2  | Reject* Ethernet packet       |                    |
| PORTB4 |                | RXCB                  | D17 † | 49   | I/O | 2  | SPI-S-CLK-I-B                 | SPI-M-CLK-O-B      |
| PORTB3 | RXDB           |                       | C17 † | 50   | I/O | 2  | SPI-S-RXD-I-B                 | SPI-M-RXD-O-B      |
| PORTB2 | DSRB*          | DAK2*                 | C16 † | 51   | I/O | 2  |                               |                    |
| PORTB1 | CTSB*          |                       | B16 † | 54   | I/O | 2  | RPSF* Ethernet frame boundary |                    |
| PORTB0 | DCDB*          | DON2*                 | A16 † | 55   | I/O | 2  |                               |                    |
| PORTC7 |                | TXCA                  | A15 † | 56   | I/O | 2  | SPI-S-EN-I-A                  | SPI-M-EN-O-A       |
| PORTC6 | RIA*           | IRQO*                 | C14 † | 57   | I/O | 2  |                               |                    |
| PORTC5 |                | TXCB                  | B15 † | 58   | I/O | 2  | SPI-S-EN-I-B                  | SPI-M-EN-O-B       |
| PORTC4 | RIB*           |                       | A14 † | 59   | I/O | 2  |                               |                    |
| PORTC3 |                | AMUX                  | D13 † | 60   | I/O | 8  | Interrupt 3                   |                    |
| PORTC2 |                |                       | C13 † | 61   | I/O | 8  | Interrupt 2                   |                    |
| PORTC1 |                |                       | B14 † | 62   | I/O | 8  | Interrupt 1                   |                    |
| PORTC0 |                |                       | B13 † | 63   | I/O | 8  | Interrupt 0                   |                    |

**ENI/Parallel 1284 Interface**

| IEEE1284 | ENI     | GPIO   | BGA   | PQFP  | I/O | OD | Description              |
|----------|---------|--------|-------|-------|-----|----|--------------------------|
| PDATA0   | PDATA0  | GPIO0  | R14 † | 200   | I/O | 2  |                          |
| PDATA1   | PDATA1  | GPIO1  | P14 † | 201   | I/O | 2  |                          |
| PDATA2   | PDATA2  | GPIO2  | U13 † | 202   | I/O | 2  |                          |
| PDATA3   | PDATA3  | GPIO3  | R15 † | 203   | I/O | 2  |                          |
| PDATA4   | PDATA4  | GPIO4  | T14 † | 204   | I/O | 2  |                          |
| PDATA5   | PDATA5  | GPIO5  | U14 † | 205 † | I/O | 2  |                          |
| PDATA6   | PDATA6  | GPIO6  | U15 † | 206   | I/O | 2  |                          |
| PDATA7   | PDATA7  | GPIO7  | T15 † | 207   | I/O | 2  |                          |
| POE1*    | PDATA8  |        | T16 † | 2     | I/O | 2  |                          |
| POE2*    | PDATA9  |        | T17 † | 3     | I/O | 2  |                          |
| POE3*    | PDATA10 |        | R17 † | 4     | I/O | 2  |                          |
| POE4*    | PDATA11 |        | P15 † | 5     | I/O | 2  |                          |
| PCLKC1   | PDATA12 |        | R16 † | 6     | I/O | 2  |                          |
| PCLKC2   | PDATA13 |        | P17 † | 7     | I/O | 2  |                          |
| PCLKC3   | PDATA14 |        | N14 † | 8     | I/O | 2  |                          |
| PCLKC4   | PDATA15 |        | N15 † | 9     | I/O | 2  |                          |
| PCLKD1   | PACK*   | GPIOF7 | G16   | 35    | I/O | 8  |                          |
| PCLKD2   | PEN*    | GPIOF6 | P16 † | 10    | I/O | 2  |                          |
| PCLKD3   | PINT1*  | GPIOF5 | N16   | 11    | I/O | 2  |                          |
| PCLKD4   | PINT2*  | GPIOF4 | M15   | 12    | I/O | 2  | Or ENI DMA output PDRQIO |
| ACK1*    | PA0     | GPIH0  | M14   | 13    | I   |    |                          |
| ACK2*    | PA1     | GPIH1  | N17   | 14    | I   |    |                          |
| ACK3*    | PA2     | GPIH2  | M16   | 15    | I   |    |                          |
| ACK4*    | PA3     | GPIH3  | L15   | 16    | I   |    |                          |
| BUSY1    | PA4     | GPIH4  | L14   | 17    | I   |    |                          |
| BUSY2    | PA5     | GPIOH5 | M17   | 18    | I   |    |                          |
| BUSY3    | PA6     | GPIH6  | L16   | 19    | I   |    |                          |
| BUSY4    | PA7     | GPIH7  | K15   | 20    | I   |    |                          |
| PE1      | PA8     | GPIG0  | K14   | 21    | I   |    |                          |
| PE2      | PA9     | GPIG1  | L17   | 22    | I   |    |                          |
| PE3      | PA10    | GPIG2  | K16   | 23    | I   |    |                          |
| PE4      | PA11    | GPIG3  | J15   | 24    | I   |    |                          |



**ENI/Parallel 1284 Interface (cont.)**

| IEEE1284 | ENI   | GPIO   | BGA | PFQFP | I/O | OD | Description              |
|----------|-------|--------|-----|-------|-----|----|--------------------------|
| PSELECT1 | PA12  | GPIG4  | J14 | 25    | I   |    |                          |
| PSELECT2 | PA13  | GPIOF3 | H15 | 28    | I/O | 2  | Or ENI DMA output PDRQI* |
| PSELECT3 | PA14  | GPIOF2 | H14 | 29    | I/O | 2  | Or ENI DMA output PDRQO* |
| PSELECT4 | PA15  | GPIG5  | J17 | 30    | I   |    | Or ENI DMA input PDACK*  |
| FAULT1*  | PA16  | GPIG6  | H16 | 31    | I   |    |                          |
| FAULT2*  | PCS*  | GPIG7  | H17 | 34    | I   |    |                          |
| FAULT3*  | PRW*  | GPIOF0 | G14 | 33    | I/O | 2  |                          |
| FAULT4*  | PBRW* | GPIOF1 | G15 | 32    | I/O | 2  |                          |

**Clock generation**

| Signal  | BGA   | PQFP | I/O | OD | Description                      |
|---------|-------|------|-----|----|----------------------------------|
| XTAL1   | U7    | 178  | I   |    | 2.5 V crystal oscillator circuit |
| XTAL2   | T8    | 179  | O   |    |                                  |
| PLLVD   | U8    | 182  |     |    | 2.5 V PLL clean power            |
| PLLLPF  | P9    | 181  |     |    | PLL loop filter capacitor        |
| PLLVSS  | R9    | 180  |     |    | PLL clean ground                 |
| PLLTST* | P8 †  | 177  | I   |    | 2.5 V PLL test mode              |
| BISTEN* | R10 † | 184  | I   |    | Enable internal BIST operation   |
| SCANEN* | P10 † | 185  | I   |    | Enable internal SCAN testing     |

**System reset**

| Signal | BGA  | PQFP | I/O | OD | Description    |
|--------|------|------|-----|----|----------------|
| RESET* | T2 † | 158  | I   |    | System reset * |

**Debug support for ARM core**

| Signal | BGA  | PQFP | I/O | OD | Description                          |
|--------|------|------|-----|----|--------------------------------------|
| TDI    | T6 † | 171  | I   |    | Test data in                         |
| TDO    | U5   | 170  | O   | 2  | Test data out                        |
| TMS    | R7 † | 172  | I   |    | Test mode select                     |
| TRST*  | R8   | 174  | I   |    | Test mode reset (input current sink) |
| TCK    | P7   | 173  | I   |    | Test mode clock                      |

## Power supply

| Signal                         | BGA                        | PQFP                      | Description                                                          |
|--------------------------------|----------------------------|---------------------------|----------------------------------------------------------------------|
| V <sub>CC</sub> DC 3.3 V DC    | F15, B17, C12, A2, M2, U9  | 36, 52, 64, 104, 143, 186 | I/O steady state (6 pairs)                                           |
| V <sub>SS</sub> DC Gnd Returns | F14, A17, D12, A1, N3, U10 | 37, 53, 65, 105, 144, 188 |                                                                      |
| V <sub>CC</sub> AC 3.3 V       | A8, E1, T1, U16            | 86, 118, 156, 208         | I/O switching (4 pairs — see note below on 3.3 V power and GND pads) |
| V <sub>SS</sub> AC Gnd Return  | B7, F2, U1, U17            | 87, 119, 157, 1           |                                                                      |
| V <sub>DD</sub> CO 2.5 V       | K17, A10, H1, T7           | 26, 78, 130, 175          | Core power (4 pairs)                                                 |
| V <sub>SS</sub> CO Gnd Returns | J16, B9, J2, U6            | 27, 79, 131, 176          |                                                                      |
| PLL V <sub>DD</sub> 2.5 V      | U8                         | 182                       | PLL bead filtered clean power                                        |
| PLL V <sub>SS</sub> Gnd Return | R9                         | 180                       | Power-up reset ground reference                                      |
| POR V <sub>SS</sub> Gnd        | T9                         | 183                       |                                                                      |

### Additional information about NET + 50 pins

- All outputs drive TTL levels. Outputs drive to 0.4 V maximum on low, 2.4 V minimum on high.
- The following pins require a 2.5 V input level:

| Signal | BGA | PQFP |
|--------|-----|------|
| XTAL1  | U7  | 178  |
| PLLTST | P8  | 177  |
| PLLVDD | U8  | 182  |

- TRST\* (R8, 174) is the only pin that is an input current sink.
- Remaining inputs are TTL levels and are 3.3 V tolerant, allowing integration with 3.3 V devices.
- Regarding 3.3 V power and GND pads: In general, you should use separate power pairs for AC and DC power to prevent the noise in the AC power buses from reaching the DC power buses. Digi recommends (and uses) a ferrite bead to filter the AC power pins.

## Registers and addresses

### General control module

| Address     | Register                  | Address     | Register                            |
|-------------|---------------------------|-------------|-------------------------------------|
| 0xFFB0 0000 | System control register   | 0xFFB0 0024 | Port B register                     |
| 0xFFB0 0004 | System status register    | 0xFFB0 0028 | Port C register                     |
| 0xFFB0 0008 | PLL control register      | 0xFFB0 0030 | Interrupt enable register           |
| 0xFFB0 000C | Software service register | 0xFFB0 0034 | Interrupt enable register — Set     |
| 0xFFB0 0010 | Timer 1 control register  | 0xFFB0 0038 | Interrupt enable register — Clear   |
| 0xFFB0 0014 | Timer 1 status register   | 0xFFB0 0034 | Interrupt status register — Enabled |
| 0xFFB0 0018 | Timer 2 control register  | 0xFFB0 0038 | Interrupt status register — Raw     |
| 0xFFB0 001C | Timer 2 status register   | 0xFFB0 0040 | Cache control register 0            |
| 0xFFB0 0020 | Port A register           | 0xFFB0 0044 | Cache control register 1            |

### Memory module controller

| Address     | Register                                    | Address     | Register                                   |
|-------------|---------------------------------------------|-------------|--------------------------------------------|
| 0xFFC0 0000 | Memory module configuration register (MMCR) | 0xFFC0 0034 | Chip select 2 option register (OR2)        |
| 0xFFC0 0010 | Chip select 0 base address register (BAR0)  | 0xFFC0 0038 | Chip select 2 option register B (OR2B)     |
| 0xFFC0 0014 | Chip select 0 option register (OR0)         | 0xFFC0 0040 | Chip select 3 base address register (BAR3) |
| 0xFFC0 0018 | Chip select 0 option register B (OR0B)      | 0xFFC0 0044 | Chip select 3 option register (OR3)        |
| 0xFFC0 0020 | Chip select 1 base address register (BAR1)  | 0xFFC0 0048 | Chip select 3 option register B (OR3B)     |
| 0xFFC0 0024 | Chip select 1 option register (OR1)         | 0xFFC0 0050 | Chip select 4 base address register (BAR4) |
| 0xFFC0 0028 | Chip select 1 option register B (OR1B)      | 0xFFC0 0054 | Chip select 4 option register (OR4)        |
| 0xFFC0 0030 | Chip select 2 base address register (BAR2)  | 0xFFC0 0058 | Chip select 4 option register B (OR4B)     |

## DMA controller module

DMA register key:  $0xFF90nnnn$  where  $nnnn = DMAx + Offset$

| DMAx:       |    |                                  |    |     |     | Offset: |                           |
|-------------|----|----------------------------------|----|-----|-----|---------|---------------------------|
| 1A:         | 00 | 2:                               | 80 | 6:  | 100 | 00      | Buffer descriptor pointer |
| 1B:         | 20 | 3:                               | A0 | 7:  | 120 | 10      | Buffer control register   |
| 1C:         | 40 | 4:                               | C0 | 8:  | 140 | 14      | Buffer status register    |
| 1D:         | 60 | 5:                               | E0 | 9:  | 160 |         |                           |
|             |    |                                  |    | 10: | 180 |         |                           |
| Examples:   |    |                                  |    |     |     |         |                           |
| 0xFF90 0000 |    | DMA 1A buffer descriptor pointer |    |     |     |         |                           |
| 0xFF90 0010 |    | DMA 1A buffer control register   |    |     |     |         |                           |
| 0xFF90 0014 |    | DMA 1A buffer status register    |    |     |     |         |                           |

## Ethernet controller module

| Address            | Register                             | Address            | Register                        |
|--------------------|--------------------------------------|--------------------|---------------------------------|
| 0xFF80 0000        | General control register             | 0xFF80 0440 – 0478 | Transmit control registers      |
| 0xFF80 0004        | General status register              | 0xFF80 0480 – 0488 | Receive control registers       |
| 0xFF80 0008        | FIFO data register                   | 0xFF80 040C0       | Link fail counter               |
| 0xFF80 000C        | FIFO last word data register         | 0xFFB0 0500        | 10 Mbit jabber counter          |
| 0xFF80 0010        | TX status register                   | 0xFFB0 0504        | 10 Mbit loss of carrier counter |
| 0xFF80 0014        | RX status register                   | 0xFFB0 0540 – 0550 | MII control registers           |
| 0xFF80 0400 – 0404 | MAC configuration and test registers | 0xFFB0 0580 – 059C | Status registers                |
| 0xFF80 0408 – 040C | PCS configuration and test registers | 0xFFB0 05C0        | SAL address filter register     |
| 0xFF80 0410 – 0414 | STL configuration and test registers | 0xFFB0 05C4 – 05DC | SAL hash table registers        |

## Serial controller module

| Address            | Register            | Address            | Register            |
|--------------------|---------------------|--------------------|---------------------|
| 0xFFD0 0000 – 0030 | Channel 1 registers | 0xFFD0 0040 – 0070 | Channel 2 registers |

## ENI controller module

| Address            | Register                             | Address            | Register                               |
|--------------------|--------------------------------------|--------------------|----------------------------------------|
| 0xFFA0 0000        | General control register             | 0xFFA0 0030        | ENI control register                   |
| 0xFFA0 0004        | General status register              | 0xFFA0 0034        | ENI pulsed interrupt register          |
| 0xFFA0 0008        | FIFO mode data register              | 0xFFA0 0038        | ENI shared RAM address register        |
| 0xFFA0 0010 – 001C | IEEE1284 ports 1–4 control registers | 0xFFA0 003C        | ENI shared register                    |
| 0xFFA0 0020 – 002C | IEEE 1284 ports 1–4 data registers   | 0xFFA0 0040 – 0050 | GPIO ports D, F, G, H, and F registers |

## Test modes and PLL usage

The PLLTST\*, BISTEN\*, and SCANEN\* primary inputs control test modes for test operations (in manufacturing) and for using an external oscillator instead of a crystal, as follows:

| PLLTST * | BISTEN * | SCANEN * | Mode                                    |
|----------|----------|----------|-----------------------------------------|
| 1        | 1        | 1        | Normal with PLL operational             |
| 0        | 1        | 1        | Normal with PLL bypass                  |
| 1        | 1        | 0        | HiZ / Tri-state (manufacturing testing) |

**Note:** All other combinations of these inputs are reserved.

### PLL

When the PLLTST\* signal is active low, the PLL is isolated, and the internal system clock is provided by the XTAL1 input (XTAL1 = SYSClk). The PLL is not programmable. If you want to use the PLL (crystal) and get a system clock of 44.236 MHz, you must use an 18.432 MHz crystal.

### HiZ/Tri-state

The NET+50 chip supports a way to tri-state all outputs. When both PLLTST\* and BISTEN\* are inactive (high) and SCANEN\* is active (low), all outputs are placed in a low current tri-state mode.

## ARM debugging features

The ARM7TDMI core contains hardware extensions for advanced debugging. These extensions facilitate development and testing of application software, operating systems, and the hardware itself.

The debug extensions let you stop the core on a given instruction fetch (break-point) or data access (watchpoint), or asynchronously by a debug request. In such cases, the ARM processor is in *debug state* so you can examine the core's internal state and the system's external state. When the examination is complete, you can restore the core and system state, and resume program execution.

The ARM processor is put into debug state by an internal functional unit called *ICEBreaker*. In debug state, the core isolates itself from the memory system. You can examine the core while all other system activities – for example, DMA operations – continue normally.

You can examine the ARM processor's internal state through the 5-pin interface for debugging. This interface lets you serially insert instructions into the core's pipe-line without using the external data bus. Therefore, in debug state, you can insert a store-multiple into the instruction pipeline to dump the contents of the processor's registers. Data can be serially shifted out without affecting the rest of the system.

## DC characteristics and other specifications

### DC inputs

| Symbol   | Characteristic                   | Conditions        | Min.           | Typical | Max. | Unit    |
|----------|----------------------------------|-------------------|----------------|---------|------|---------|
| $V_{DD}$ | DC supply voltage — core         |                   | 2.25           | 2.5     | 2.75 | V       |
| $V_{CC}$ | DC supply voltage — I/O          |                   | 3.0            | 3.3     | 3.6  | V       |
| $V_{IH}$ | Input high voltage               |                   | 2.0            |         | 3.6  | V       |
| $V_{IL}$ | Input low voltage                |                   | $V_{SS} - 0.3$ |         | 0.8  | V       |
| $I_{IL}$ | Input buffer                     | $V_{IN} = V_{CC}$ | -10            |         | 10   | $\mu A$ |
|          | Input buffer with current sink   |                   | 99             |         | 429  |         |
| $I_{IH}$ | Input buffer                     | $V_{IN} = V_{SS}$ | -10            |         | 10   | $\mu A$ |
|          | Input buffer with current source |                   | 130            |         | 352  |         |
| $C_{IN}$ | Input capacitance                | Any input         | 7              |         |      | pF      |
| $V_T$    | Switching threshold              | Any input         | 1.4            | 2.0     |      | V       |

**DC outputs**

| Symbol   | Characteristic               | Conditions                                  | Min. | Max.     | Unit    |
|----------|------------------------------|---------------------------------------------|------|----------|---------|
| $V_{OL}$ | Output low voltage           |                                             | 0    | 0.4      | V       |
| $V_{OH}$ | Output high voltage          |                                             | 2.4  | $V_{CC}$ | V       |
| $I_{OZ}$ | High-Z leakage current       | $V_O = V_{SS}$                              | -10  | 10       | $\mu A$ |
| $I_{OS}$ | Output short circuit current | $V_{CC} = 3.6V, V_O (\text{low}) = V_{CC}$  |      | 55       | $\mu A$ |
|          |                              | $V_{CC} = 3.6V, V_O (\text{high}) = V_{SS}$ | -55  |          |         |
| $C_{IO}$ | Input/output capacitance     | Any input, output, or I/O                   | 7    |          | pF      |

**DC absolute maximum voltages**

| Characteristic              | Min. | Max. |
|-----------------------------|------|------|
| Supply voltage 2.5 V — core | -0.3 | 3.15 |
| Supply voltage 3.3 V — I/O  | -0.3 | 4.00 |
| Input voltage               | -0.3 | 4.50 |
| Output voltage              | -0.3 | 4.50 |

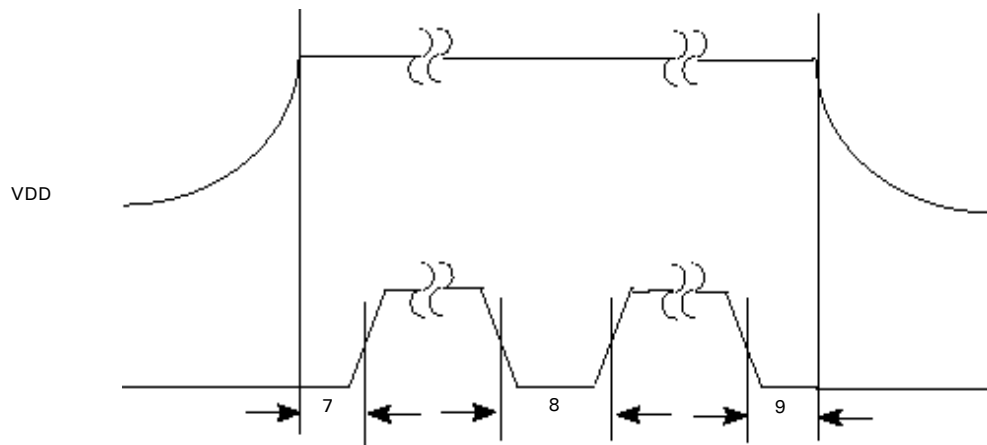
**Temperature considerations**

| Characteristic                           | Min.   | Max. |
|------------------------------------------|--------|------|
| Thermal resistance — junction to ambient | 37°C/W |      |
| Operating junction temperature (°C)      | -40°   | 100° |
| Operating ambient temperature (°C)       | -40°   | 85°  |
| Storage temperature (°C)                 | -60°   | 150° |

## Timing data and diagrams

### Reset timing

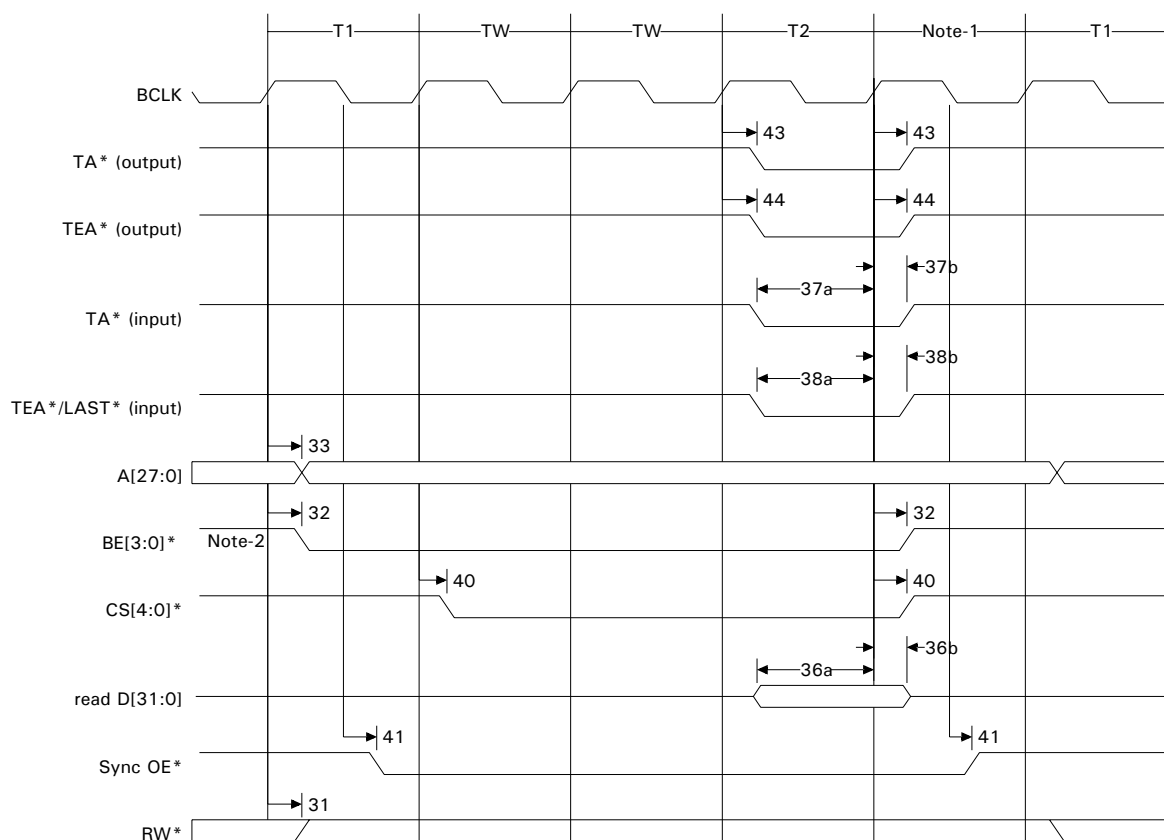
| Number | Characteristic                     | Min.            | Max. | Unit    |
|--------|------------------------------------|-----------------|------|---------|
| 7      | $V_{DD}$ at 3.0 V to RESET* high   | 40              |      | ms      |
| 8      | RESET* pulse width low             | $10/F_{SYSCLK}$ |      | $\mu s$ |
| 9      | RESET* low to $V_{DD}$ below 3.0 V | $8/F_{SYSCLK}$  |      | $\mu s$ |



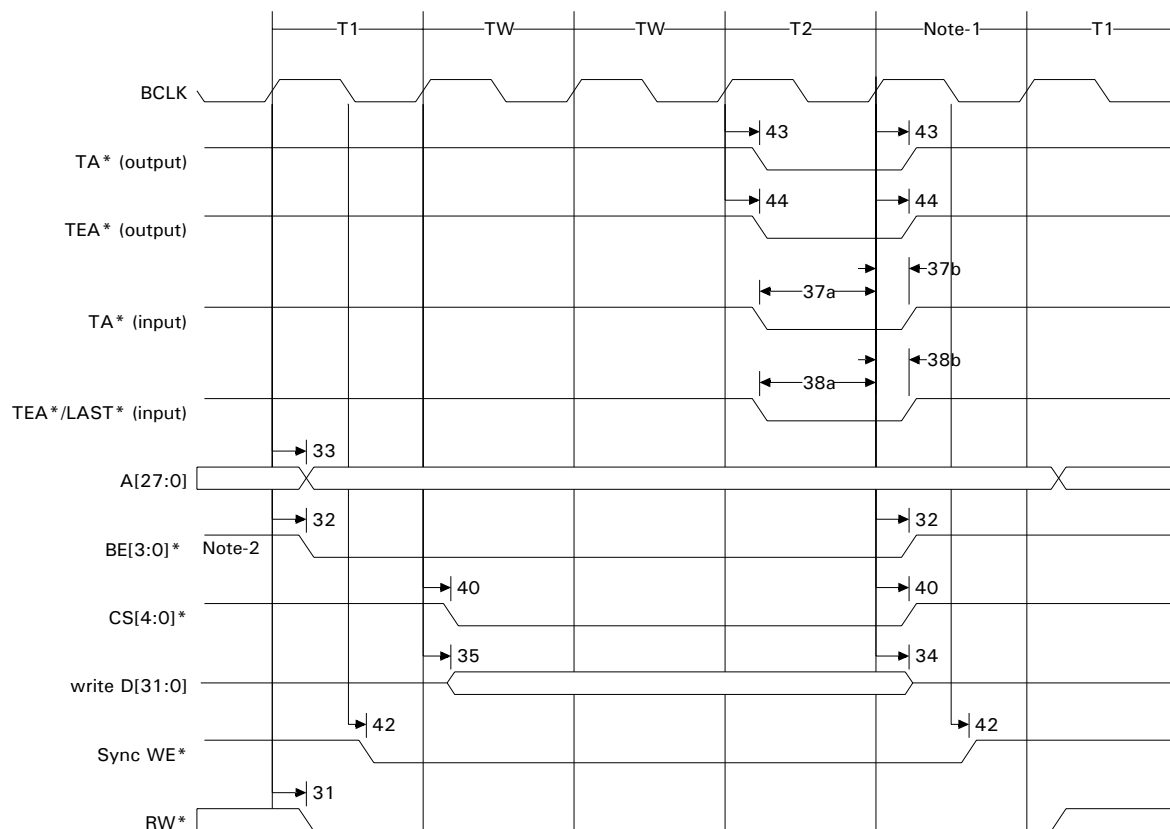


**SRAM timing**

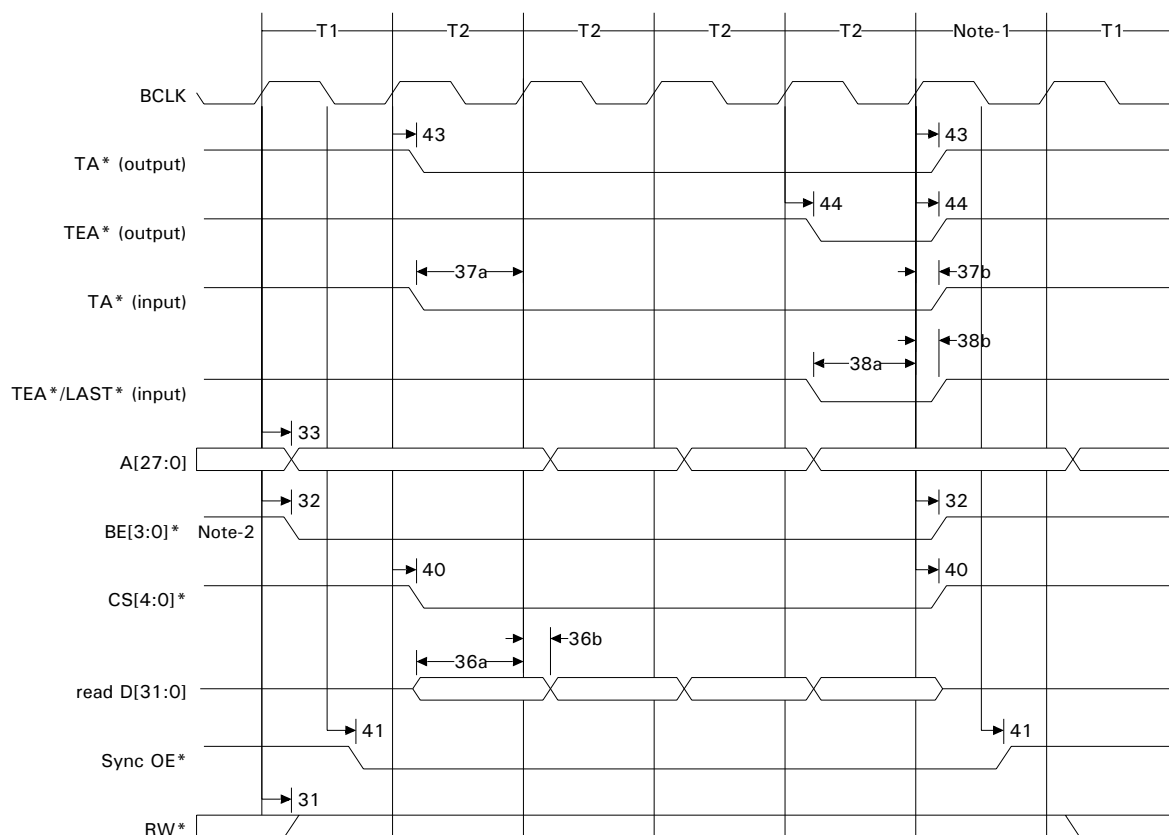
| Number                                       | Characteristic                       | Min. | Max. |
|----------------------------------------------|--------------------------------------|------|------|
| 31                                           | BCLK high to RW* valid               |      | 19   |
| 32                                           | BCLK high to BE* valid               |      | 16   |
| 33                                           | BCLK high to Address valid           | 4    | 15   |
| 34                                           | BCLK high to Data Out high impedance |      | 17   |
| 35                                           | BCLK high to Data Out valid          |      | 18   |
| 36a                                          | Data In valid to BCLK high (setup)   | 8    |      |
| 36b                                          | BCLK high to Data In invalid (hold)  | 0    |      |
| 37a                                          | TA* valid to BCLK high (setup)       | 8    |      |
| 37b                                          | BCLK high to TA* invalid (hold)      | 0    |      |
| 38a                                          | TEA* valid to BCLK high (setup)      | 8.5  |      |
| 38b                                          | BCLK high to TEA* invalid (hold)     | 0    |      |
| 40                                           | BCLK high to CS* valid               |      | 16   |
| 41                                           | BCLK low to OE* valid                |      | 14   |
| 42                                           | BCLK low to WE* valid                |      | 16   |
| 43                                           | BCLK high to TA* valid               |      | 11   |
| 44                                           | BCLK high to TEA* valid              |      | 14   |
| Minimum and maximum are in nanoseconds (ns). |                                      |      |      |

**SRAM Sync Read (Wait = 2)****Notes:**

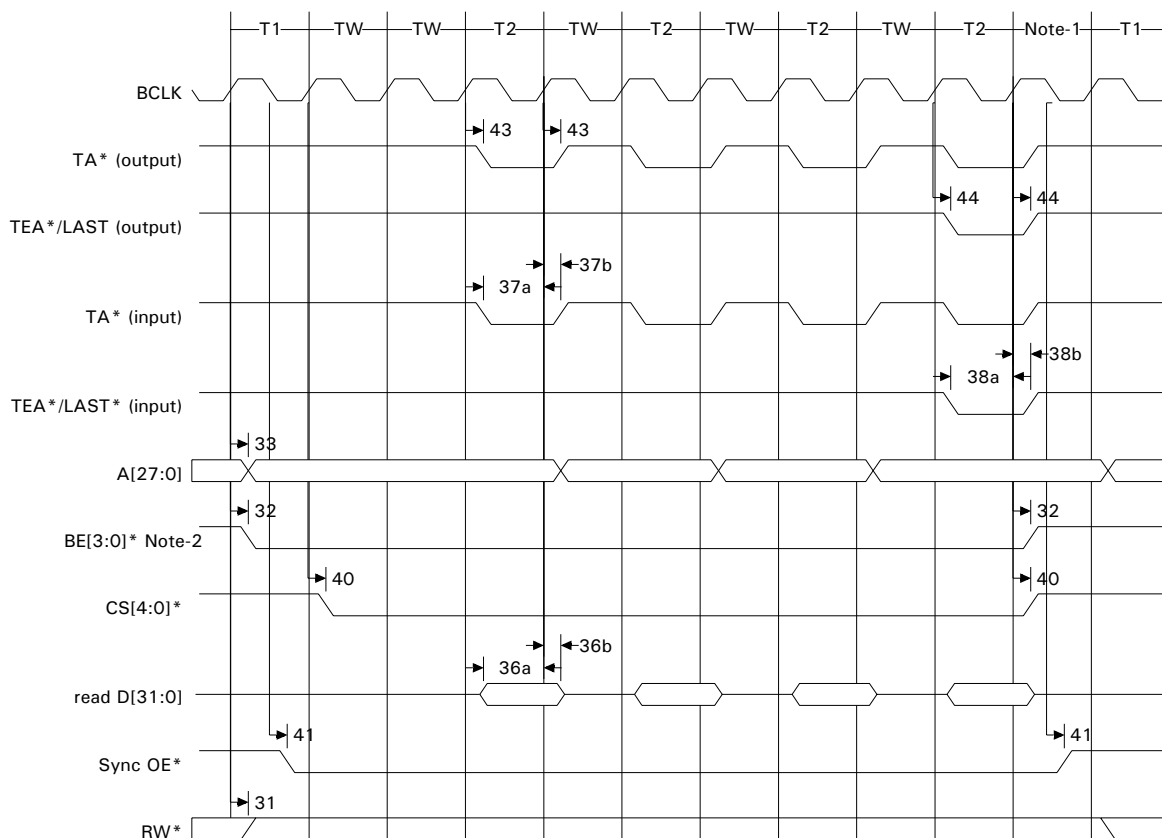
- 1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.
- 2 Port size determines which byte enable signals are active:  
 8-bit port = BE3\*  
 16-bit port = BE[3:2]\*  
 32-bit port = BE[3:0]\*

**SRAM Sync Write (Wait = 2)****Notes:**

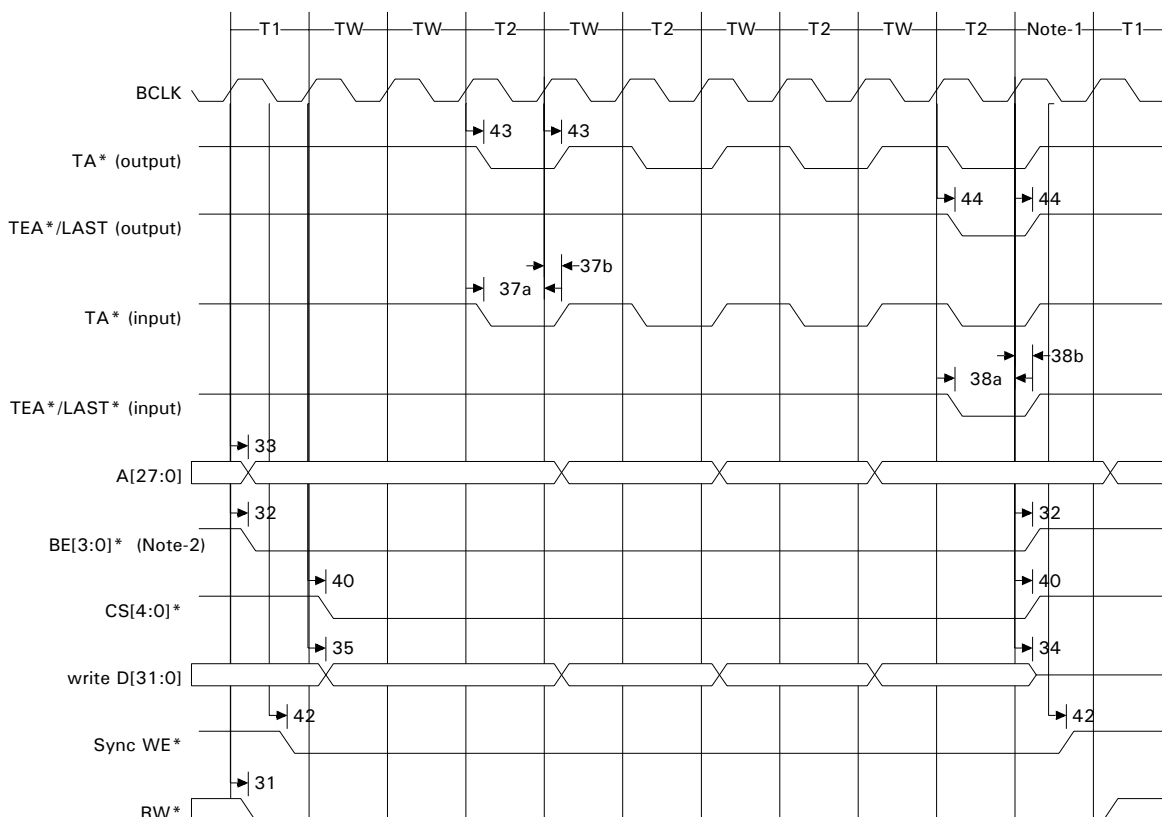
- 1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.
- 2 Port size determines which byte enable signals are active:  
 8-bit port = BE3\*  
 16-bit port = BE[3:2]\*  
 32-bit port = BE[3:0]\*

**SRAM Sync Burst Read (2-111, Wait = 0, BCYC = 00)****Notes:**

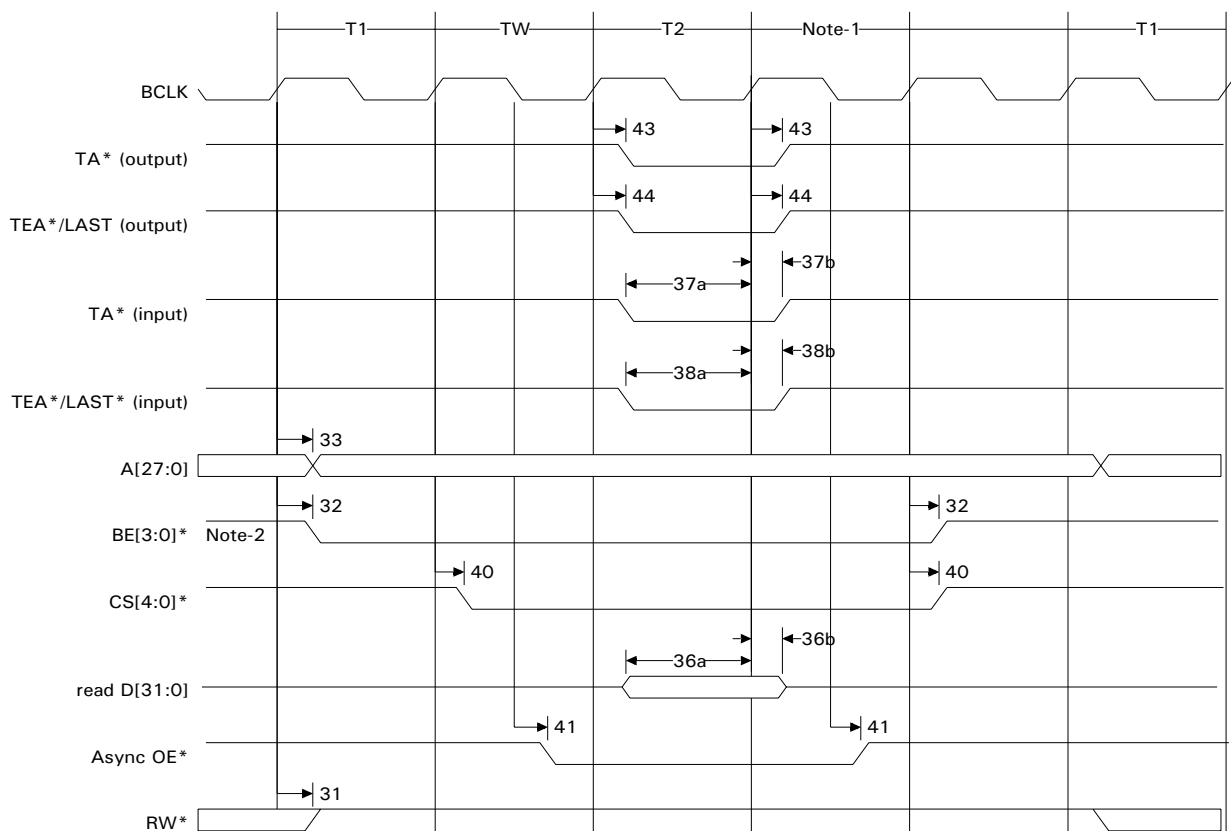
- 1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.
- 2 Port size determines which byte enable signals are active:  
 8-bit port = BE3\*  
 16-bit port = BE[3:2]\*  
 32-bit port = BE[3:0]\*

**SRAM Sync Burst Read (4-222, Wait = 2, BCYC = 01)****Notes:**

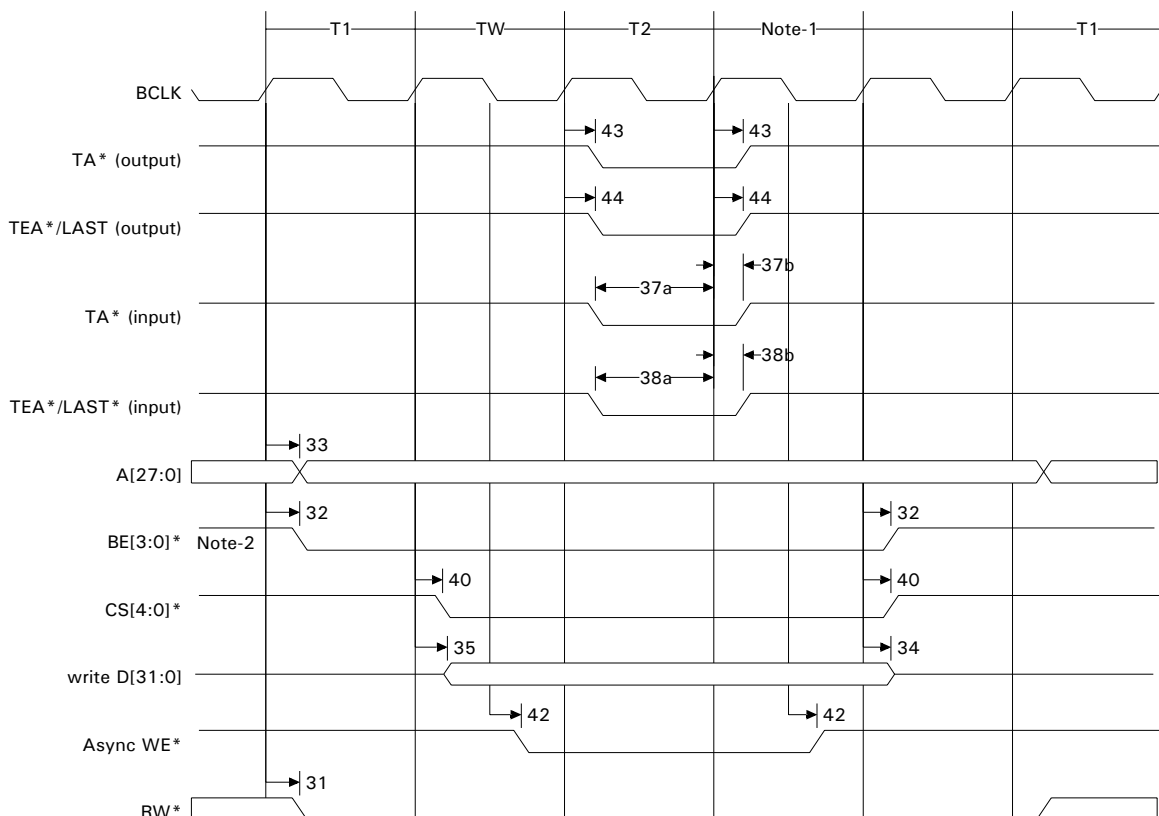
- 1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.
- 2 Port size determines which byte enable signals are active:  
 8-bit port = BE3\*  
 16-bit port = BE[3:2]\*  
 32-bit port = BE[3:0]\*

**SRAM Sync Burst Write (4-222, Wait = 2, BCYC = 01)****Notes:**

- 1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.
- 2 Port size determines which byte enable signals are active:  
 8-bit port = BE3\*  
 16-bit port = BE[3:2]\*  
 32-bit port = BE[3:0]\*

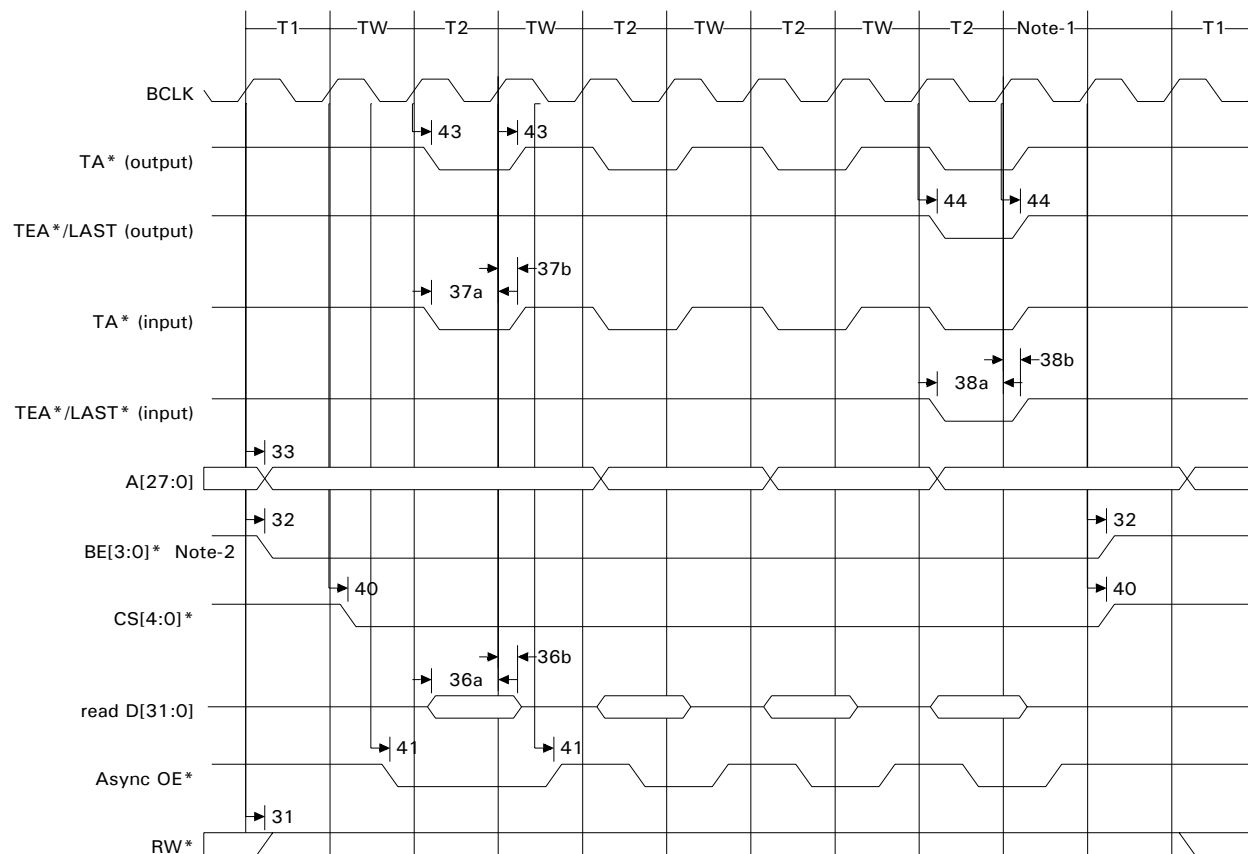
**SRAM Async Read (Wait = 2)****Notes:**

- 1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.
- 2 Port size determines which byte enable signals are active:  
 8-bit port = BE3\*  
 16-bit port = BE[3:2]\*  
 32-bit port = BE[3:0]\*
- 3 The TW cycles are present when the WAIT field is set to 2 or more.

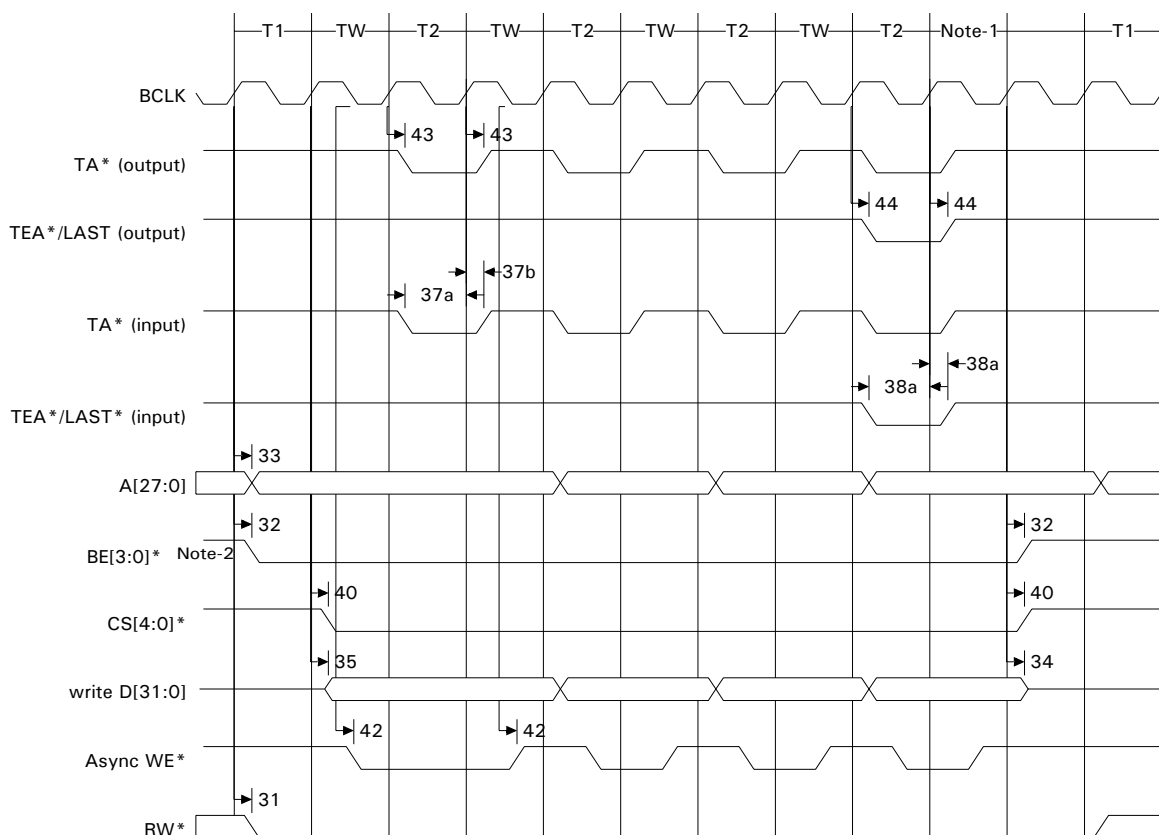
**SRAM Async Write (Wait = 2)****Notes:**

- 1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.
- 2 Port size determines which byte enable signals are active:  
 8-bit port = BE3\*  
 16-bit port = BE[3:2]\*  
 32-bit port = BE[3:0]\*
- 3 The TW cycles are present when the WAIT field is set to 2 or more.



**SRAM Async Burst Read (Wait = 2, BCYC = 01)****Notes:**

- 1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.
- 2 Port size determines which byte enable signals are active:  
 8-bit port = BE3\*  
 16-bit port = BE[3:2]\*  
 32-bit port = BE[3:0]\*
- 3 The TW cycles are present when the WAIT field is set to 2 or more.

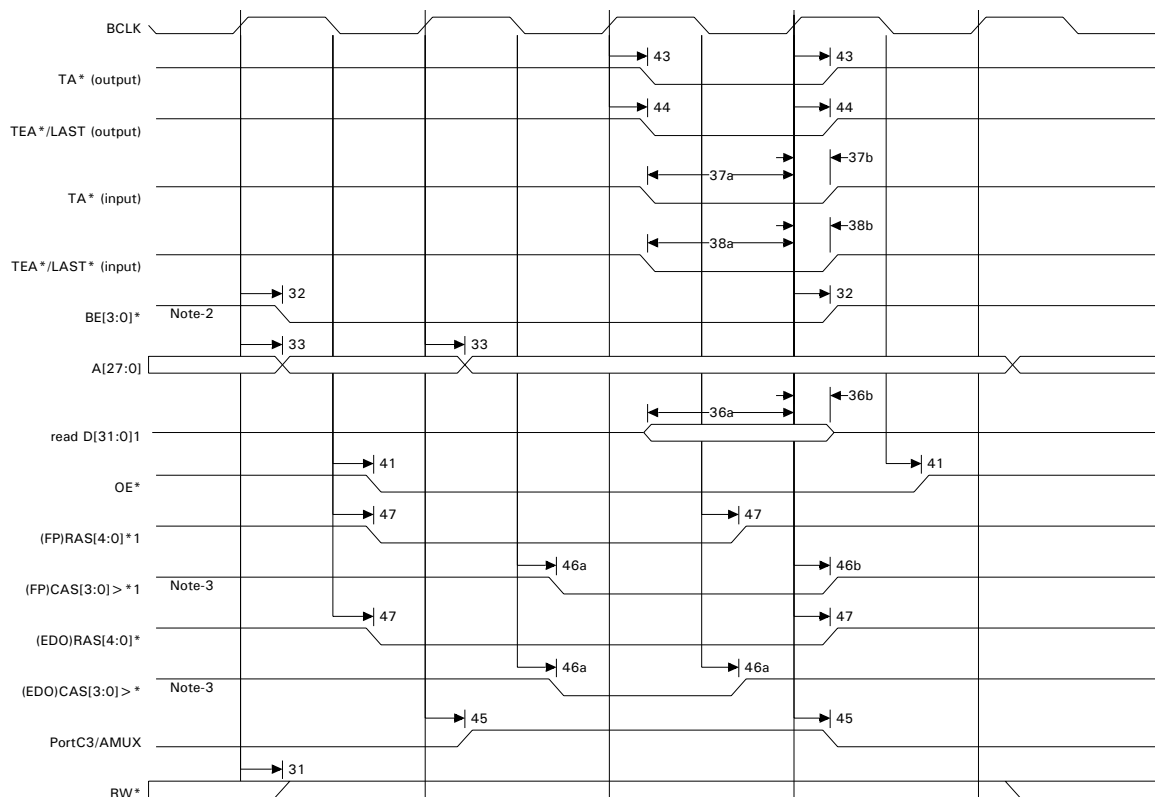
**SRAM Async Burst Write (Wait = 2, BCYC = 01)****Notes:**

- 1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.
- 2 Port size determines which byte enable signals are active:  
 8-bit port = BE3\*  
 16-bit port = BE[3:2]\*  
 32-bit port = BE[3:0]\*
- 3 The TW cycles are present when the WAIT field is set to 2 or more.

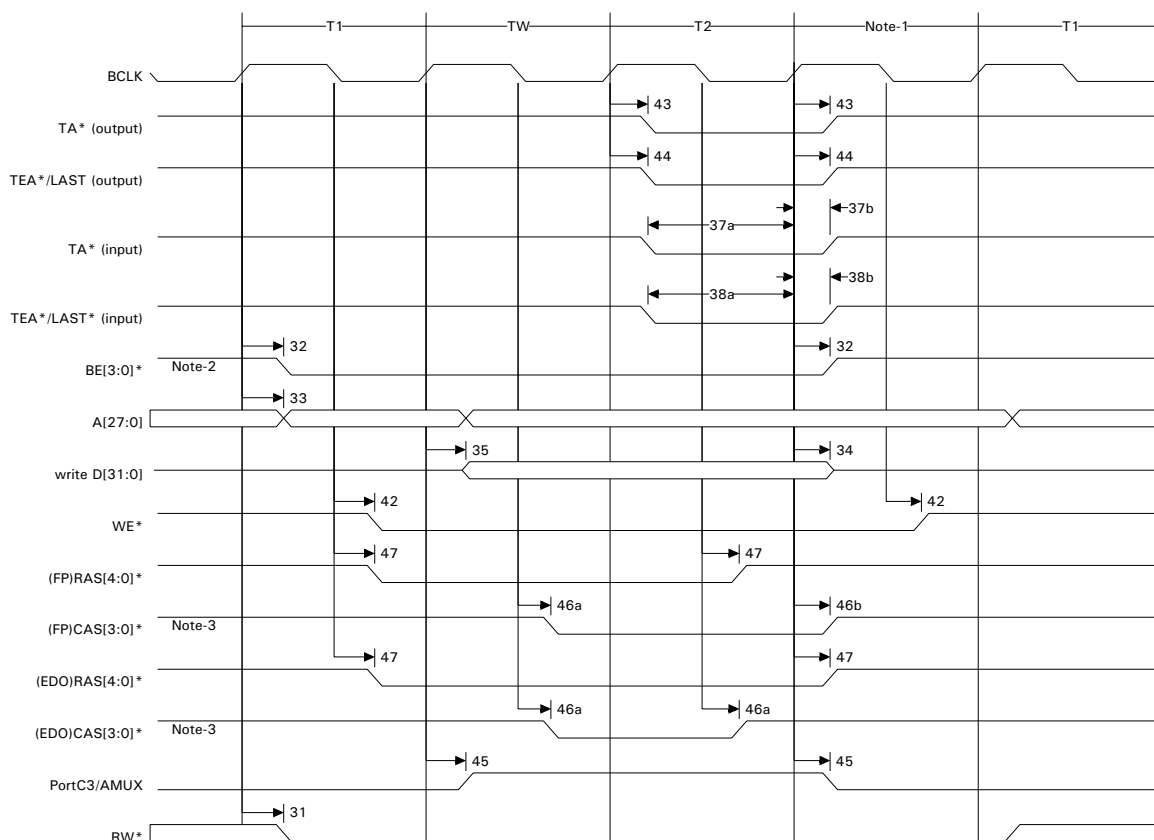
**Fast Page and EDO DRAM timing**

| Number | Characteristic                       | Min. | Max. |
|--------|--------------------------------------|------|------|
| 31     | BCLK high to RW* valid               |      | 19   |
| 32     | BCLK high to BE* valid               |      | 16   |
| 33     | BCLK high to Address valid           | 4    | 15   |
| 34     | BCLK high to Data Out high impedance |      | 17   |
| 35     | BCLK high to Data Out valid          |      | 18   |
| 36a    | Data In valid to BCLK high (setup)   | 8    |      |
| 36b    | BCLK high to Data In invalid (hold)  | 0    |      |
| 37a    | TA* valid to BCLK high (setup)       | 8    |      |
| 37b    | BCLK high to TA* invalid (hold)      | 0    |      |
| 38a    | TEA* valid to BCLK high (setup)      | 8.5  |      |
| 38b    | BCLK high to TEA* invalid (hold)     | 0    |      |
| 41     | BCLK low to OE* valid                |      | 14   |
| 42     | BCLK low to WE* valid                |      | 16   |
| 43     | BCLK high to TA* valid               |      | 11   |
| 44     | BCLK high to TEA* valid              |      | 14   |
| 45     | BCLK high to PORTC3/AMUX valid       |      | 8    |
| 46a    | BCLK low to CAS* valid               |      | 13   |
| 46b    | BCLK high to CAS* valid              |      | 13   |
| 47     | BCLK low to RAS* valid               |      | 16   |

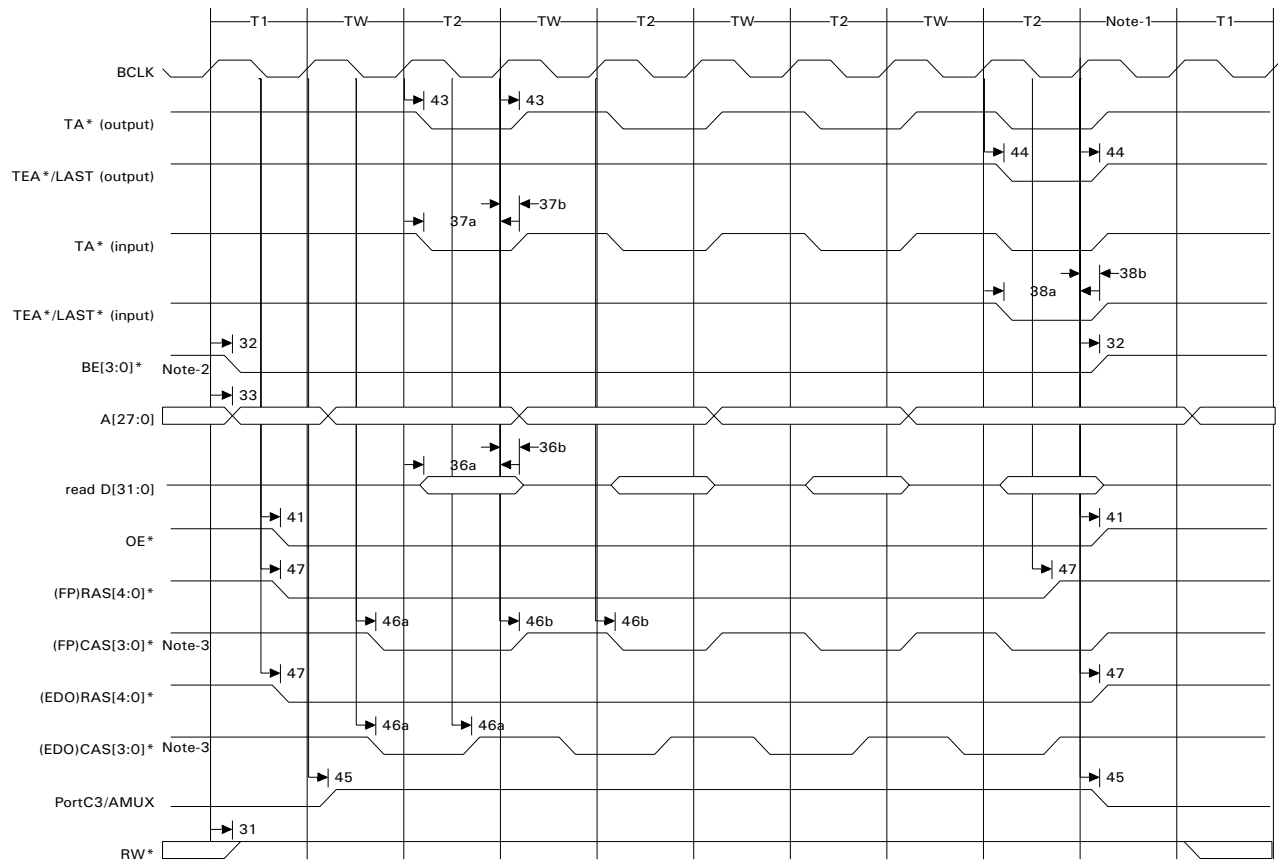
Minimum and maximum are in nanoseconds (ns).

**Fast Page and EDO DRAM Read****Notes:**

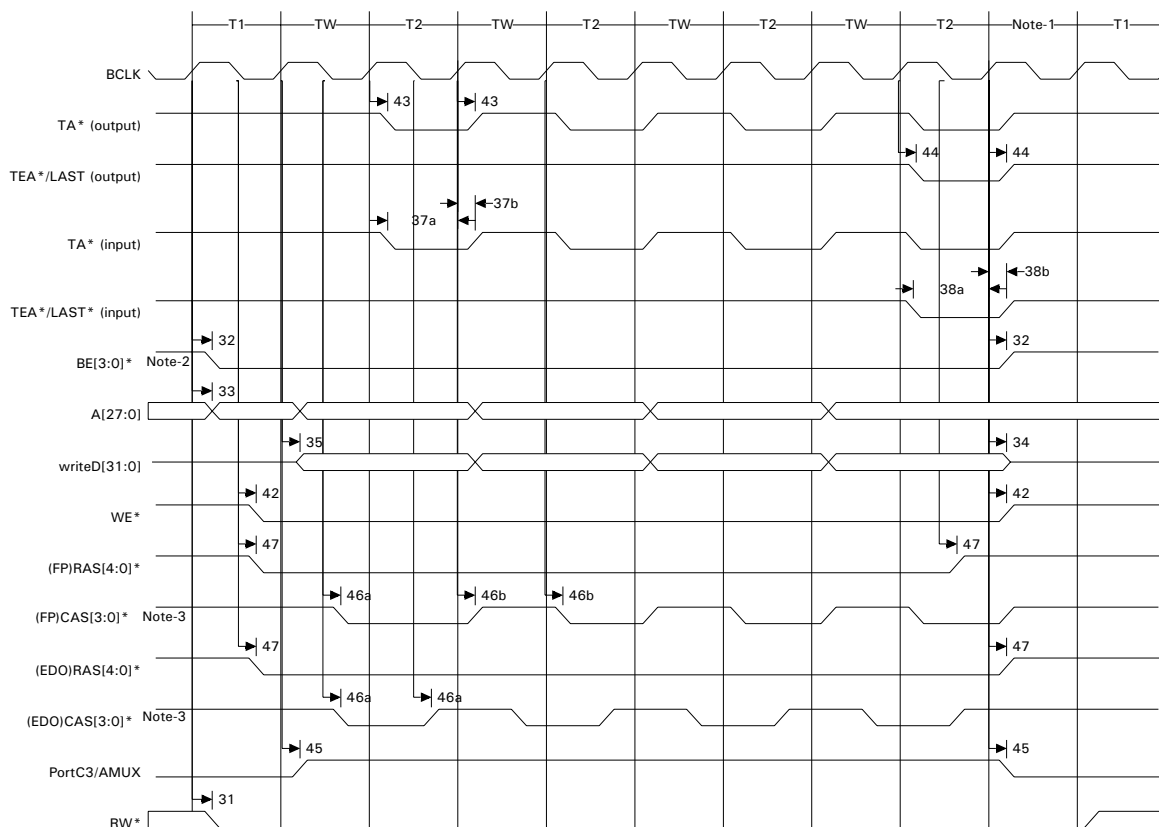
- 1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.
- 2 Port size determines which byte enable signals are active:  
 8-bit port = BE3\*  
 16-bit port = BE[3:2]\*  
 32-bit port = BE[3:0]\*
- 3 Port size determines which CAS\* signals are active:  
 8-bit port = CAS3\*  
 16-bit port = CAS[3:2]\*  
 32-bit port = CAS[3:0]\*

**Fast Page and EDO DRAM Write****Notes:**

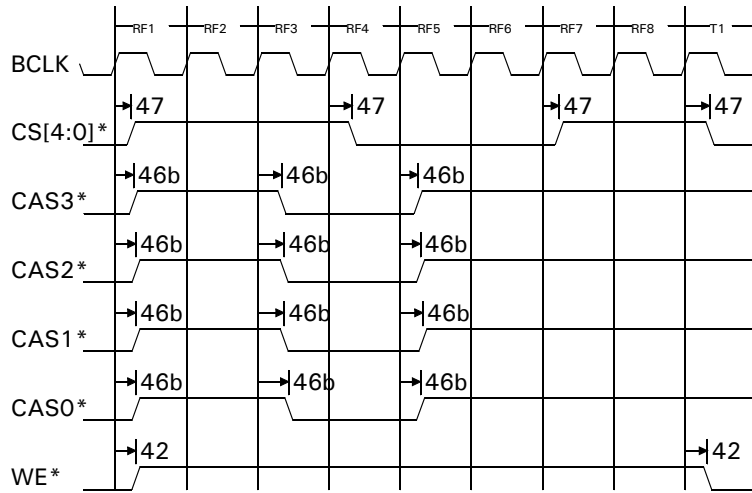
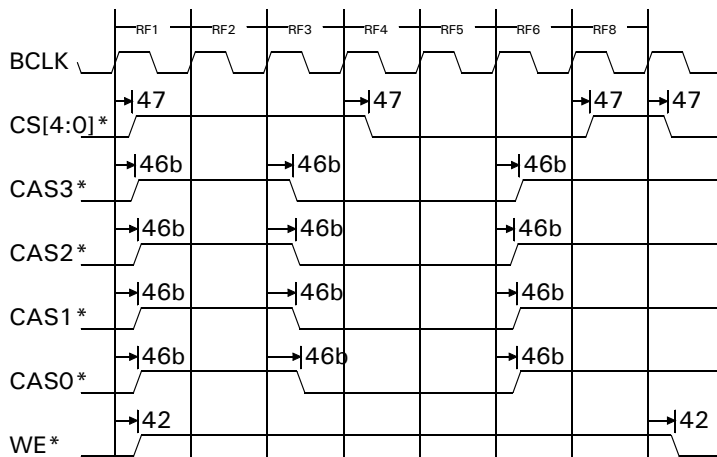
- 1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.
- 2 Port size determines which byte enable signals are active:  
 8-bit port = BE3\*  
 16-bit port = BE[3:2]\*  
 32-bit port = BE[3:0]\*
- 3 Port size determines which CAS\* signals are active:  
 8-bit port = CAS3\*  
 16-bit port = CAS[3:2]\*  
 32-bit port = CAS[3:0]\*

**Fast Page and EDO DRAM Burst Read****Notes:**

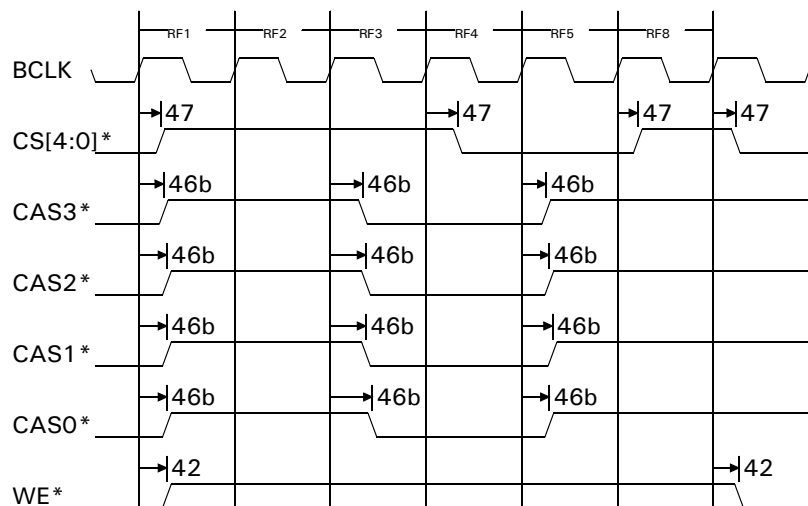
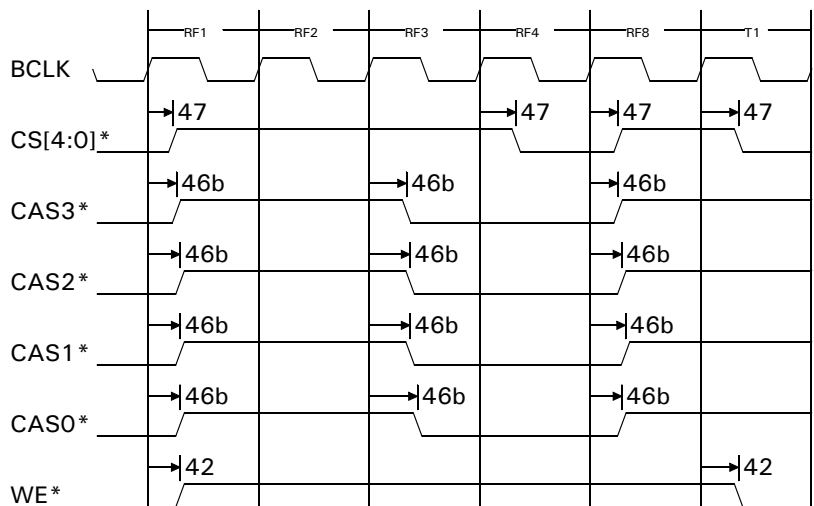
- 1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.
- 2 Port size determines which byte enable signals are active:  
 8-bit port = BE3\*  
 16-bit port = BE[3:2]\*  
 32-bit port = BE[3:0]\*
- 3 Port size determines which CAS\* signals are active:  
 8-bit port = CAS3\*  
 16-bit port = CAS[3:2]\*  
 32-bit port = CAS[3:0]\*
- 4 The BCYC field in the Chip Select Option register should never be set to 00 for Fast Page and EDO DRAM.

**Fast Page and EDO DRAM Burst Write****Notes:**

- 1 There can be 0, 1, or 2 null periods between memory transfers. Contact the factory for details.
- 2 Port size determines which byte enable signals are active:  
 8-bit port = BE3\*  
 16-bit port = BE[3:2]\*  
 32-bit port = BE[3:0]\*
- 3 Port size determines which CAS\* signals are active:  
 8-bit port = CAS3\*  
 16-bit port = CAS[3:2]\*  
 32-bit port = CAS[3:0]\*
- 4 The BCYC field in the Chip Select Option register should never be set to 00 for Fast Page and EDO DRAM.

**Fast Page and EDO DRAM Refresh (RCYC = 0)****Fast Page and EDO DRAM Refresh (RCYC = 1)**

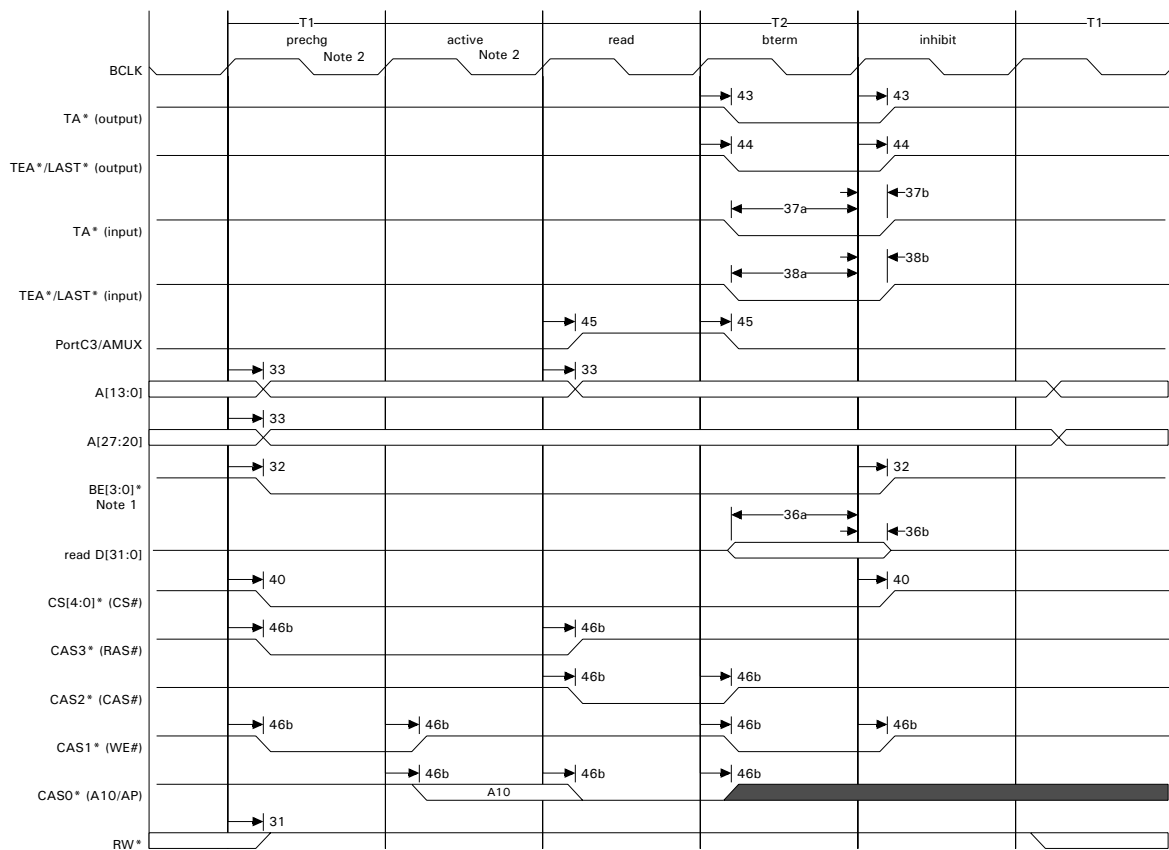


**Fast Page and EDO DRAM Refresh (RCYC = 2)****Fast Page and EDO DRAM Refresh (RCYC = 3)**

**SDRAM timing**

| Number | Characteristic                       | Min. | Max. |
|--------|--------------------------------------|------|------|
| 31     | BCLK high to RW* valid               |      | 19   |
| 32     | BCLK high to BE* valid               |      | 16   |
| 33     | BCLK high to Address valid           | 4    | 15   |
| 34     | BCLK high to Data Out high impedance |      | 17   |
| 35     | BCLK high to Data Out valid          |      | 18   |
| 36a    | Data In valid to BCLK high (setup)   | 8    |      |
| 36b    | BCLK high to Data In invalid (hold)  | 0    |      |
| 37a    | TA* valid to BCLK high (setup)       | 8    |      |
| 37b    | BCLK high to TA* invalid (hold)      | 0    |      |
| 38a    | TEA* valid to BCLK high (setup)      | 8.5  |      |
| 38b    | BCLK high to TEA* invalid (hold)     | 0    |      |
| 40     | BCLK high to CS* valid               |      | 16   |
| 41     | BCLK low to OE* valid                |      | 14   |
| 42     | BCLK low to WE* valid                |      | 16   |
| 43     | BCLK high to TA* valid               |      | 11   |
| 44     | BCLK high to TEA* valid              |      | 14   |

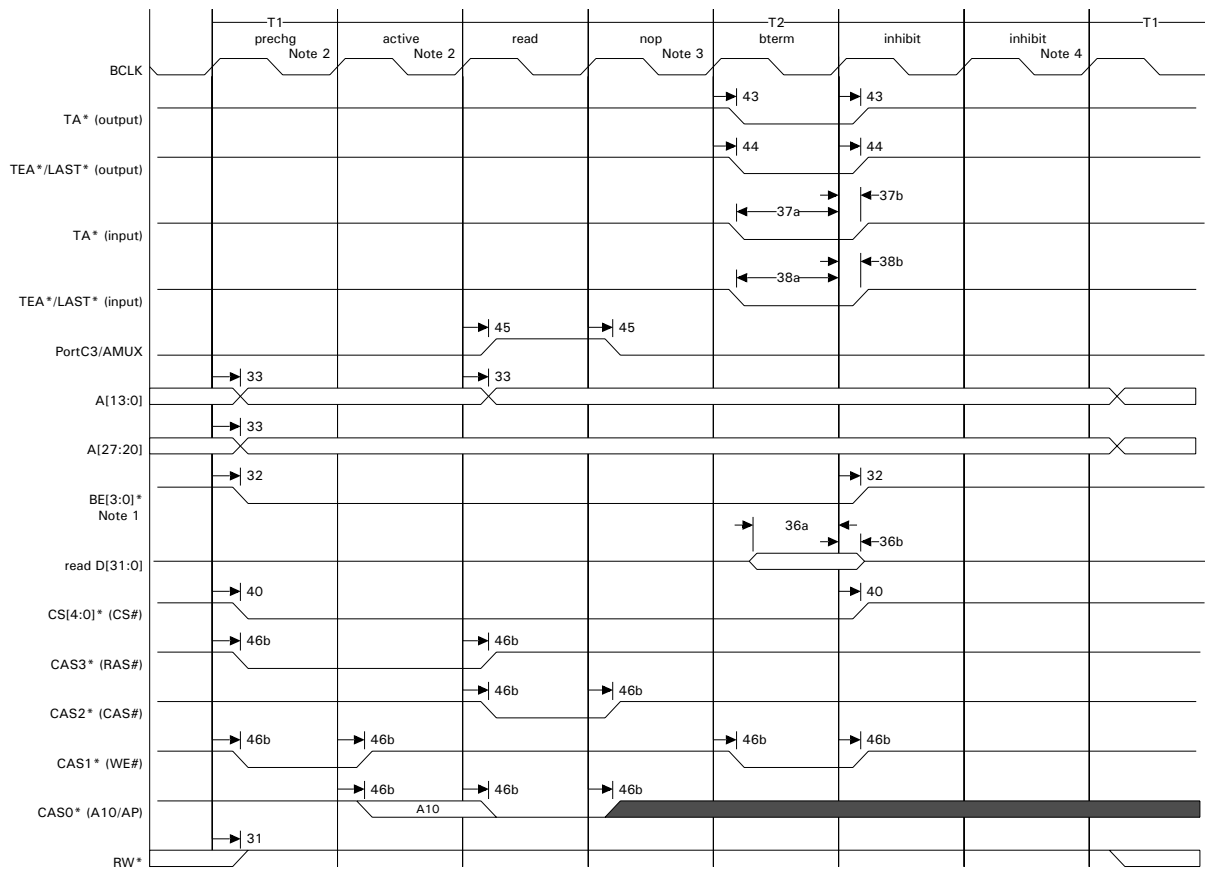
Minimum and maximum are in nanoseconds (ns).

**SDRAM Read (CAS Latency = 1)**

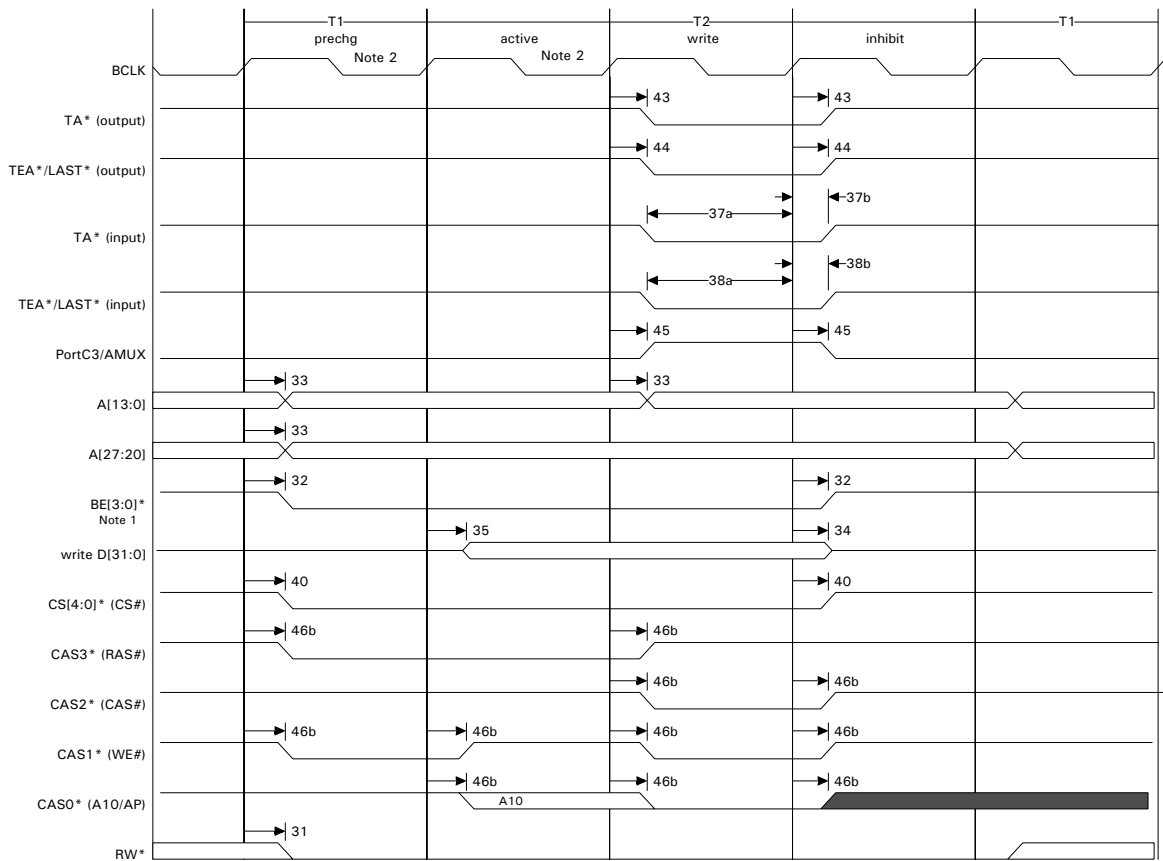
Note 1 Port Size determines which Byte Enable signals are active

**Notes:**

- Port size determines which byte enable signals are active:
  - 8-bit port = BE3\*
  - 16-bit port = BE[3:2]\*
  - 32-bit port = BE[3:0]\*
- The Precharge command or Active command or both are not always present. They depend on the address of the previous SDRAM access.

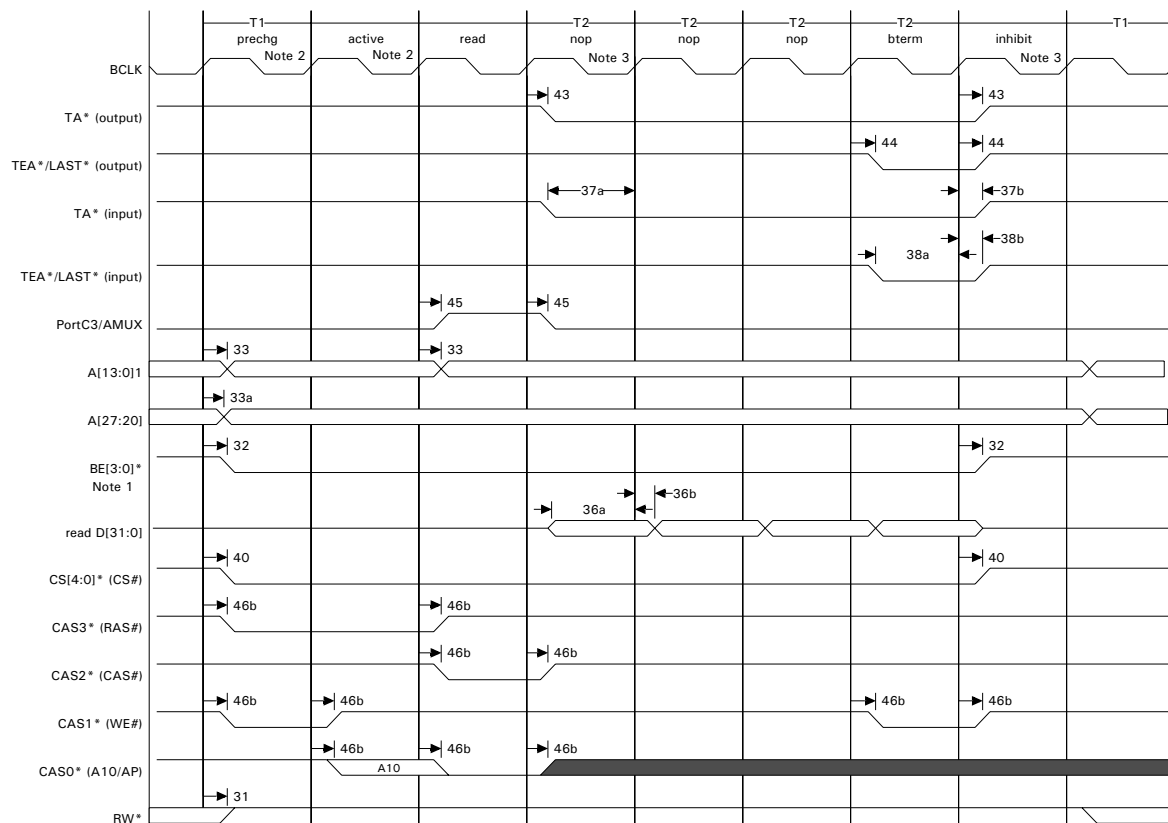
**SDRAM Read (CAS Latency = 2)****Notes:**

- 1 Port size determines which byte enable signals are active:
  - 8-bit port = BE3\*
  - 16-bit port = BE[3:2]\*
  - 32-bit port = BE[3:0]\*
- 2 The Precharge command or Active command or both are not always present. They depend on the address of the previous SDRAM access.
- 3 If CAS latency = 3, there are:
  - Two NOPs between the Read and Burst Terminate commands
  - Three Inhibit commands after the Burst Terminate command

**SDRAM Write****Notes:**

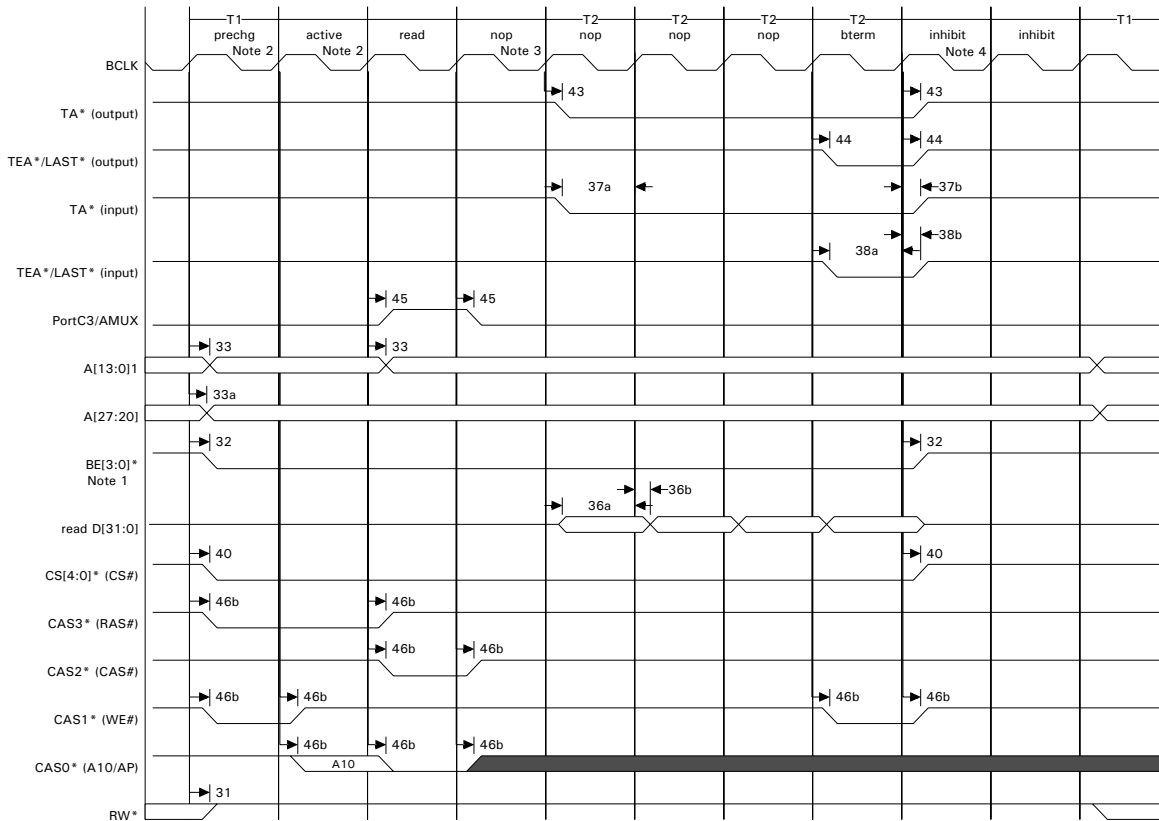
- Port size determines which byte enable signals are active:  
 8-bit port = BE3\*  
 16-bit port = BE[3:2]\*  
 32-bit port = BE[3:0]\*
- The Precharge command or Active command or both are not always present. They depend on the address of the previous SDRAM access. When the Active command is not present, parameter 35 (write D[31:0]) is not valid until the Write (T2) cycle.

***SDRAM Burst Read (CAS Latency = 1)***

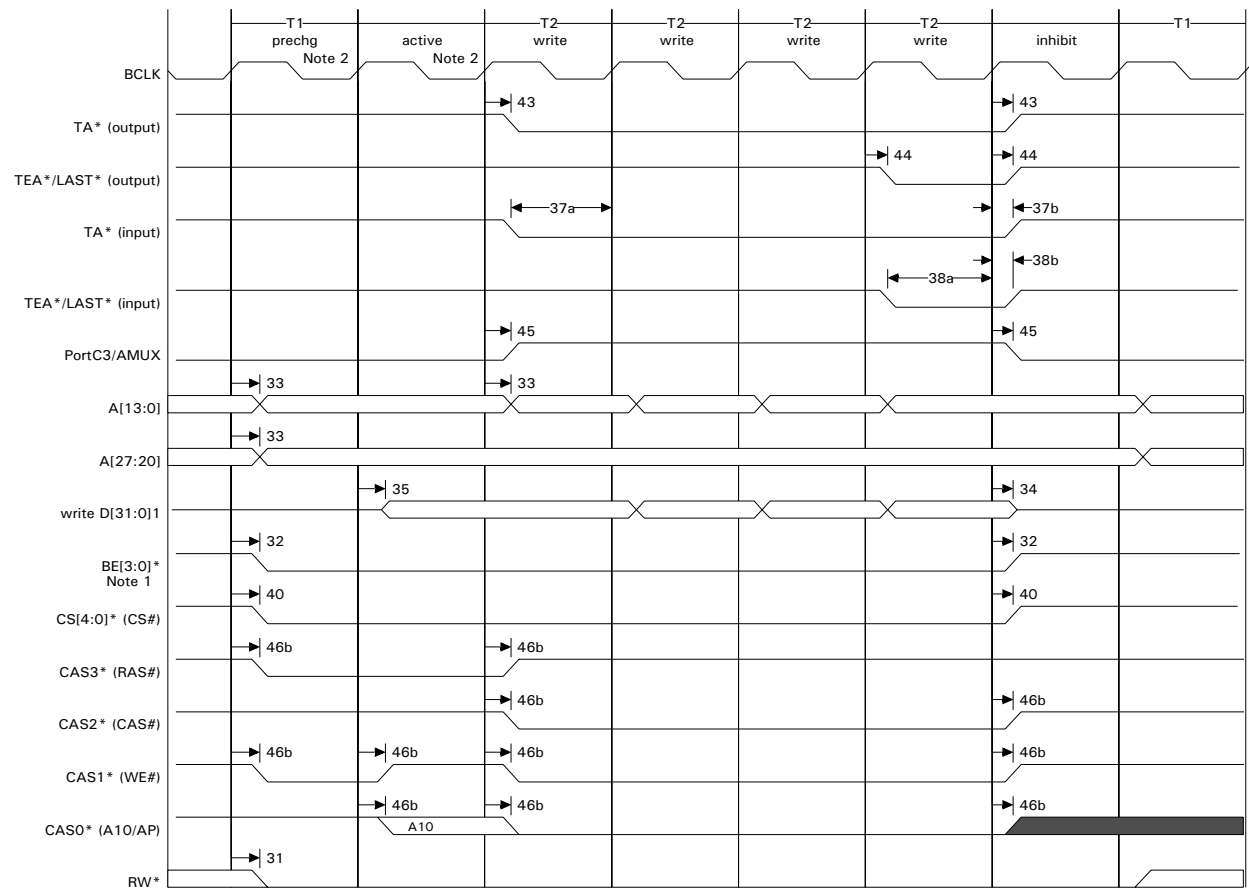


**Notes:**

- 1 Port size determines which byte enable signals are active:  
8-bit port = BE3\*  
16-bit port = BE[3:2]\*  
32-bit port = BE[3:0]\*
- 2 The Precharge command or Active command or both are not always present. They depend on the address of the previous SDRAM access.
- 3 If CAS latency = 3, there are:
  - Two NOPs between the Read and Burst Terminate commands
  - Three Inhibit commands after the Burst Terminate command

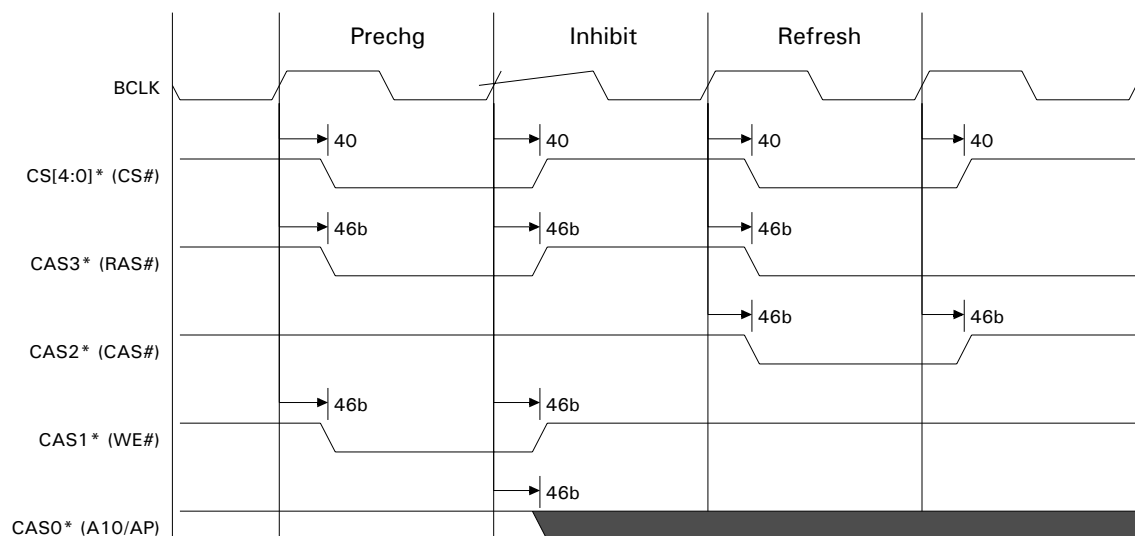
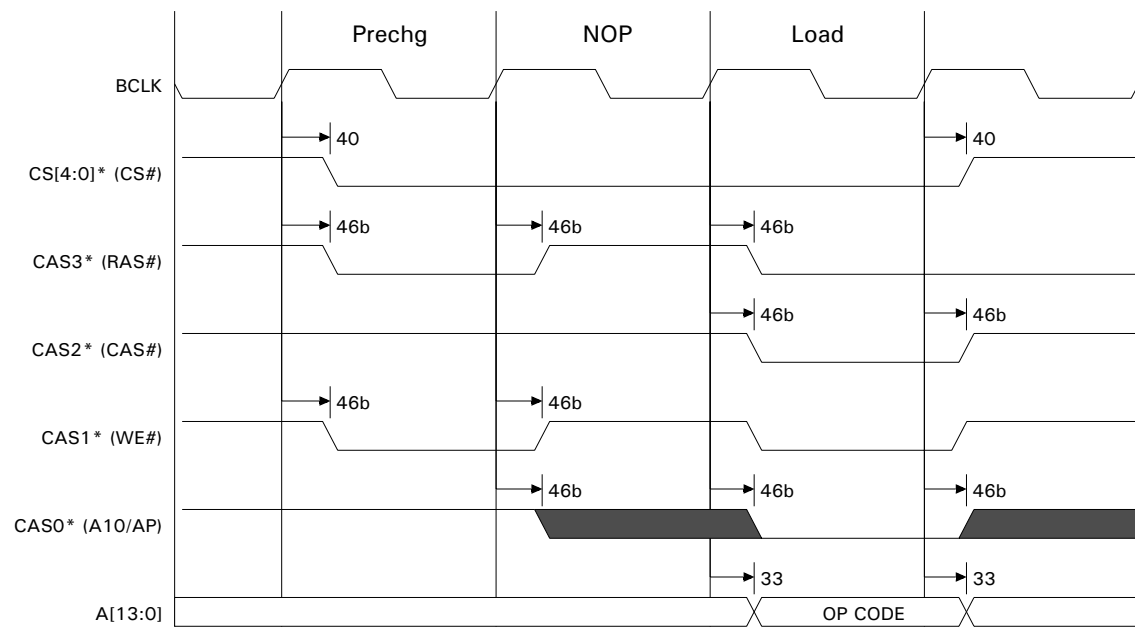
**SDRAM Burst Read (CAS Latency = 2)****Notes:**

- 1 Port size determines which byte enable signals are active:
  - 8-bit port = BE3\*
  - 16-bit port = BE[3:2]\*
  - 32-bit port = BE[3:0]\*
- 2 The Precharge command or Active command or both are not always present. They depend on the address of the previous SDRAM access.
- 3 If CAS latency = 3, there are:
  - 5 NOPs between the Read and Burst Terminate commands
  - 3 Inhibit commands after the Burst Terminate command

**SDRAM Burst Write****Notes:**

- Port size determines which byte enable signals are active:  
 8-bit port = BE3\*  
 16-bit port = BE[3:2]\*  
 32-bit port = BE[3:0]\*
- The Precharge command or Active command or both are not always present. They depend on the address of the previous SDRAM access. When the Active command is not present, parameter 35 (write D[31:0]) is not valid until the Write (T2) cycle.



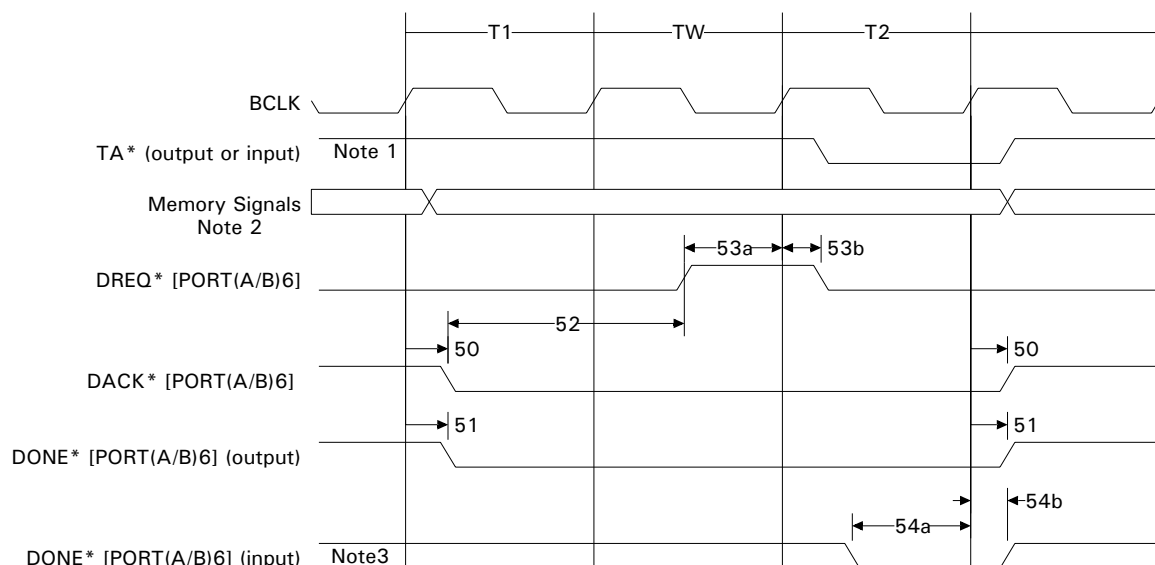
**SDRAM Refresh Command****SDRAM Load Mode Command**

## External DMA timing

| Number | Characteristic                           | Min. | Max. |
|--------|------------------------------------------|------|------|
| 50     | BCLK High to DACK* valid                 |      | 26   |
| 51     | BCLK High to DONE* (output) valid        |      | 27   |
| 52     | DACK* low to DREQ* high                  | 0    |      |
| 53a    | DREQ* valid to BCLK high (setup)         | 11   |      |
| 53b    | BCLK high to DREQ* valid (hold)          | 0    |      |
| 54a    | DONE* (input) valid to BCLK high (setup) | 14   |      |
| 54b    | BCLK high to DONE* (input) valid (hold)  | 0    |      |

Minimum and maximum are in nanoseconds (ns).

## External Fly-By DMA



### Notes:

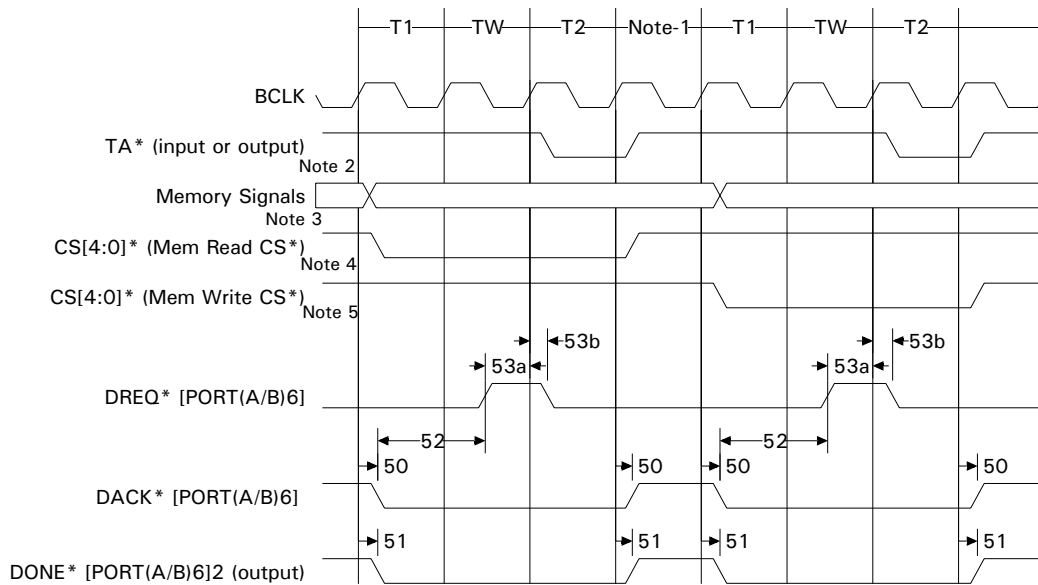
1 TA\* is shown here for reference. Its timing is available on the diagrams referenced on page 46.

2 The memory signals consist of:

|            |              |             |
|------------|--------------|-------------|
| DATA[31:0] | CS/RAS[4:0]* | OE*         |
| ADDR[27:0] | CAS[3:0]*    | WE*         |
| BE[3:0]*   | RW*          | PORTC3/AMUX |

The timing of these signals depends on how the memory is configured. See the timing diagrams referenced on page 46.

3 The DONE\* signal works as an input only when the DMA channel is configured as Fly-By Write.

**External Memory to Memory DMA****Notes:**

- 1 Between memory cycles, 0, 1, or 2 null periods can occur. Contact the factory for details.
- 2 TA\* is shown here for reference. Its timing is available on the diagrams in the sections referenced below.

**3 The memory signals consist of:**

|            |              |             |
|------------|--------------|-------------|
| DATA[31:0] | CS/RAS[4:0]* | OE*         |
| ADDR[27:0] | CAS[3:0]*    | WE*         |
| BE[3:0]*   | RW*          | PORTC3/AMUX |

The timing of these signals depends on how the memory is configured. See the timing diagrams in the sections referenced below.

- 4 The timing of the chip select associated with the buffer descriptor's source address depends on how that chip select is configured.
- 5 The timing of the chip select associated with the buffer descriptor's destination address depends on how that chip select is configured.

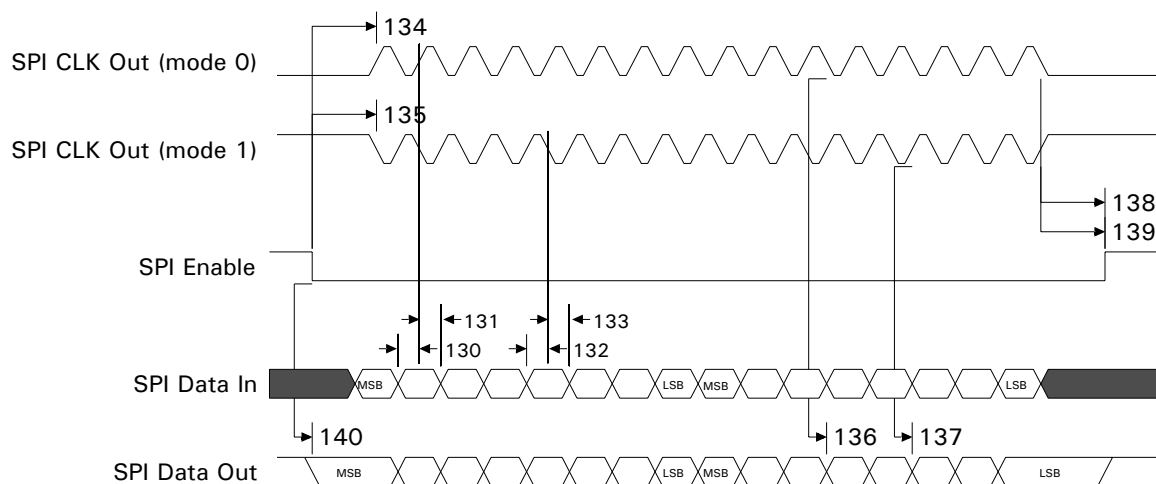
**See also**

- ["SRAM timing" on page 20](#)
- ["Fast Page and EDO DRAM timing" on page 30](#)
- ["SDRAM timing" on page 37](#)

## SPI master and slave timing

### SPI Master Mode 0 and 1 (Two-Byte Transfer)

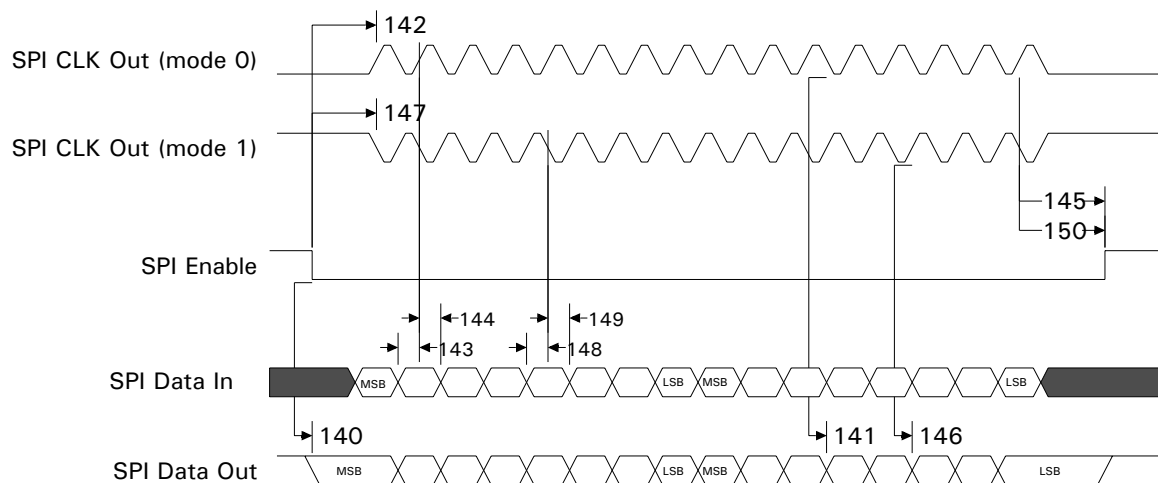
| Number | Characteristic                                | Min.  | Max. | Unit     |
|--------|-----------------------------------------------|-------|------|----------|
| 130    | Data In valid to mode 0 rising clock (setup)  | 20    |      | ns       |
| 131    | Mode 0 rising clock to Data In valid (hold)   | 0     |      | ns       |
| 132    | Data In valid to mode 1 falling clock (setup) | 20    |      | ns       |
| 133    | Mode 1 falling clock to Data In valid (hold)  | 0     |      | ns       |
| 134    | Enable low to mode 0 first rising clock       |       | 1.5  | Bit-Time |
| 135    | Enable low to mode 1 first falling clock      |       | 1.5  | Bit-Time |
| 136    | Mode 0 falling edge to Data Out valid         | -Tsys | Tsys | ns       |
| 137    | Mode 1 rising edge to Data Out valid          | -Tsys | Tsys | ns       |
| 138    | Mode 0 last falling clock to Enable high      |       | 1.5  | Bit-Time |
| 139    | Mode 1 last rising clock to Enable high       |       | 1.5  | Bit-Time |
| 140    | Enable low to Data Out valid                  | -Tsys | Tsys | ns       |



**SPI Slave Mode 0 and 1 (Two-Byte Transfer)**

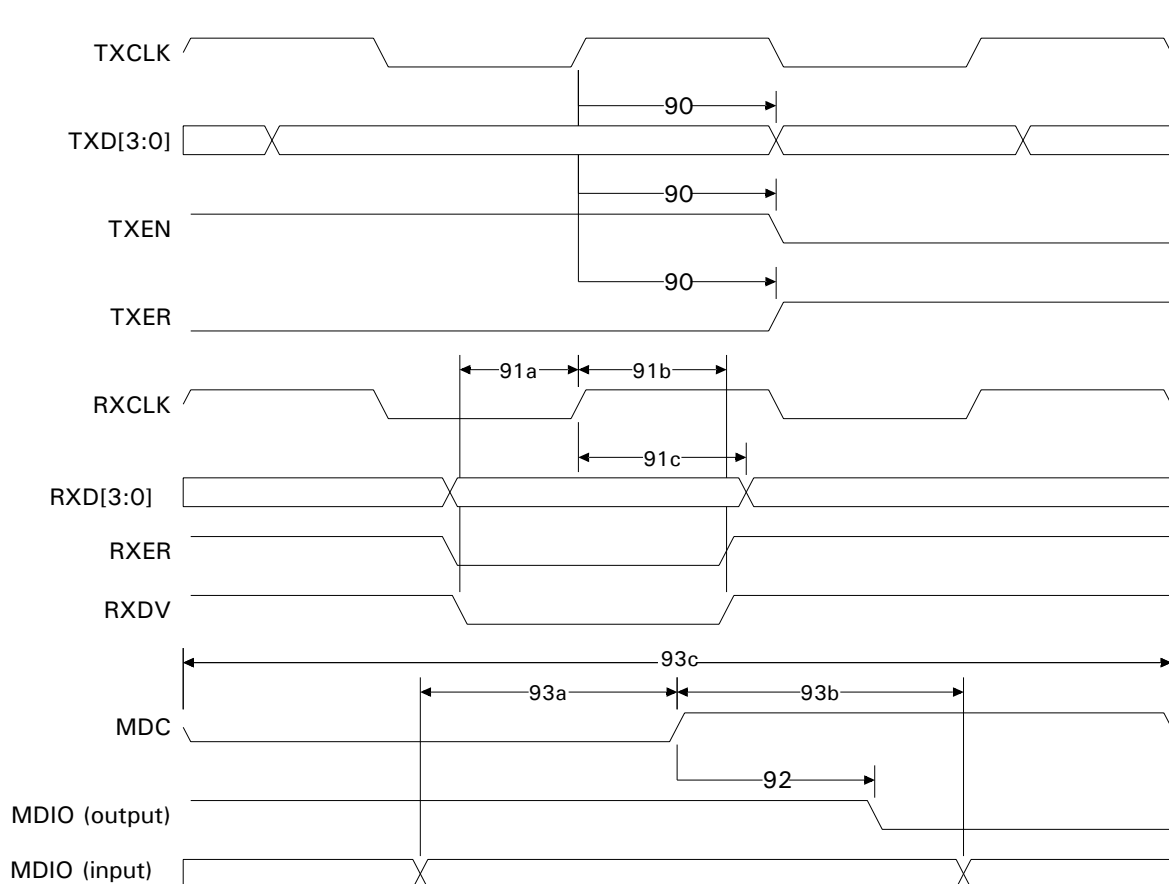
| Number | Characteristic                                   | Min.          | Max.          |
|--------|--------------------------------------------------|---------------|---------------|
| 141    | Mode 0 SPI Clock high to TXD valid               | $3 * T_{SYS}$ | $4 * T_{SYS}$ |
| 142    | Mode 0 SPI Enable low to SPI Clock high (setup)  | 0             |               |
| 143    | Mode 0 RXD Input valid to SPI Clock high (setup) | 3.4           |               |
| 144    | Mode 0 SPI Clock high to RXD input change (hold) | $4 * T_{SYS}$ |               |
| 145    | Mode 0 SPI Clock high to SPI Enable high (hold)  | $4 * T_{SYS}$ |               |
| 146    | Mode 1 SPI Clock low to TXD valid                | $3 * T_{SYS}$ | $4 * T_{SYS}$ |
| 147    | Mode 1 SPI Enable low to SPI Clock low (setup)   | 0             |               |
| 148    | Mode 1 RXD Input valid to SPI Clock low (setup)  | 3.4           |               |
| 149    | Mode 1 SPI Clock low to RXD input change (hold)  | $4 * T_{SYS}$ |               |
| 150    | Mode 1 SPI Clock low to SPI Enable high (hold)   | $4 * T_{SYS}$ |               |

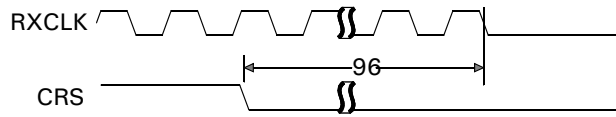
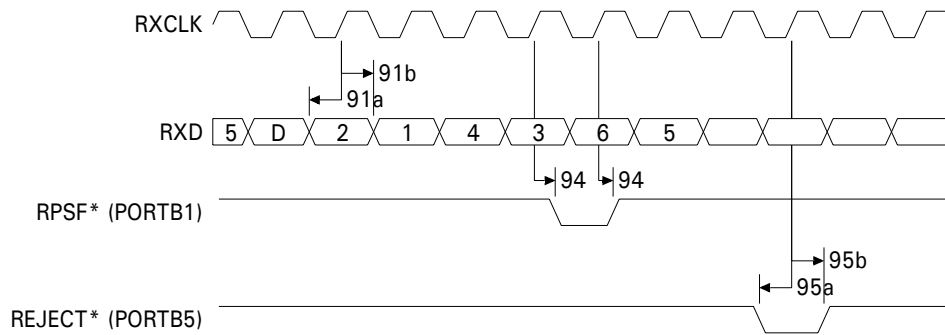
Minimum and maximum are in nanoseconds (ns).



## Ethernet timing

| Number | Characteristic                              | Min. | Max.      | Unit     |
|--------|---------------------------------------------|------|-----------|----------|
| 90     | TXCLK high to TXD, TXEN, TXER valid         | 5    | 17        | ns       |
| 91a    | RXD, RXER, RXDV valid to RXCLK high (setup) | 8    |           | ns       |
| 91b    | RXCLK high to RXD, RXER, RXDV hold time     | 0    |           | ns       |
| 91c    | RXCLK high to RXD hold time                 | 0    |           | ns       |
| 92     | MDC high to MDIO change                     | 40   | 50        | ns       |
| 93a    | MDIO valid to MDC high (setup)              | 10   |           | ns       |
| 93b    | MDC high to MDIO hold time                  | 0    |           | ns       |
| 93c    | MDC cycle time                              |      | SYSCLK/10 |          |
| 94     | RXCLK high to RPSF* change                  |      | 6.5       | ns       |
| 95a    | REJECT* valid to RXCLK high (setup)         | 2.6  |           | ns       |
| 95b    | REJECT* valid from RXCLK high (hold)        | 0    |           | ns       |
| 96     | CRS low to RXCLK idle                       | 27   |           | Bit-Time |



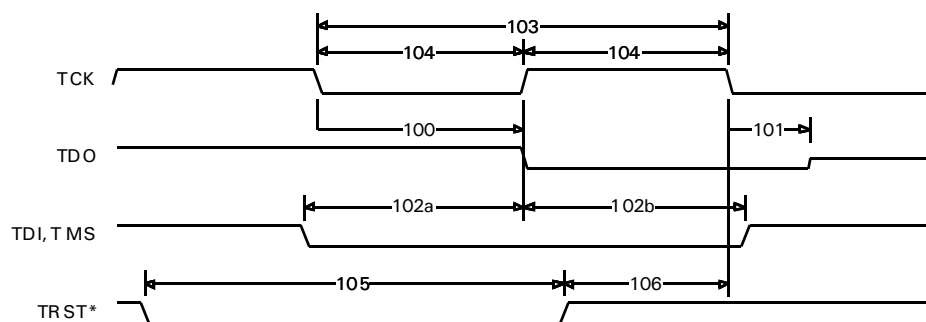
**Ethernet Receive Clock Idle****External Ethernet CAM Filtering**

## ARM core debug timing

| Number | Characteristic                     | Min. | Max. |
|--------|------------------------------------|------|------|
| 100    | TCK low to TDO valid               | 0    | 33.5 |
| 101    | TCK low to TDO high impedance      | 0    | 32.3 |
| 102a   | TDI, TMS valid to TCK high (setup) | 0.72 |      |
| 102b   | TCK high to TDI, TMS hold time     | 1.3  |      |
| 103    | TCK cycle time                     | 31.2 |      |
| 104    | TCK pulse width                    | 15.6 |      |
| 105    | TRST* low time                     | 27   |      |

Minimum and maximum are in nanoseconds (ns).

**Note:** TRST\* has an internal current sink. On production units, do not leave TRST\* pulled low. The noise margin on inputs at a logic 0 is only a few tenths of a volt. Digi recommends tying TRST\* to RESET\* on production units.





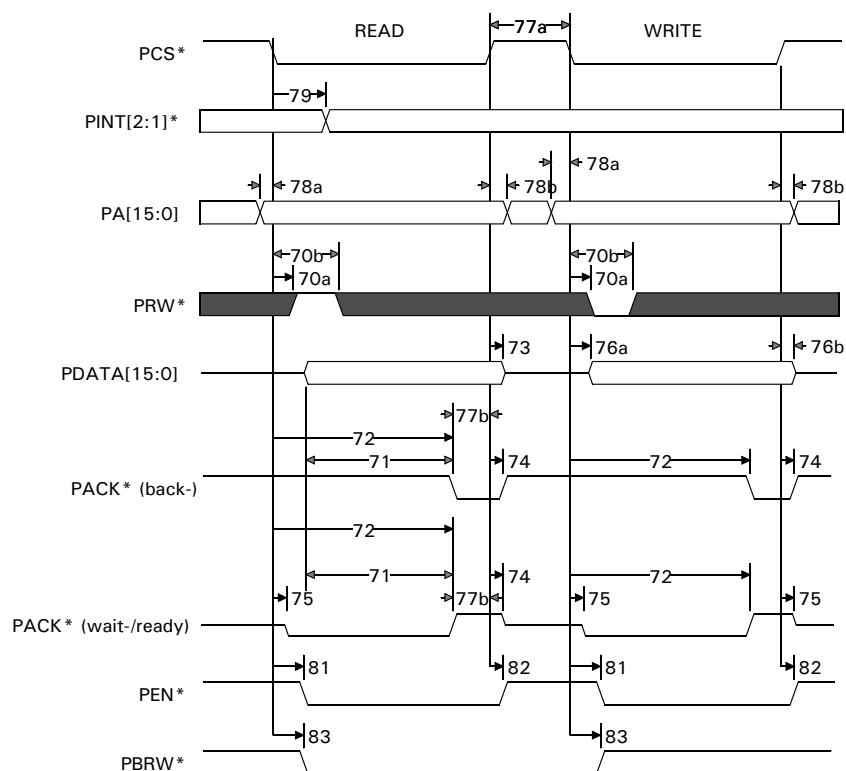
**ENI timing**

The data shown is independent of SYS\_CLK and BCLK settings. Units are nanoseconds (ns).

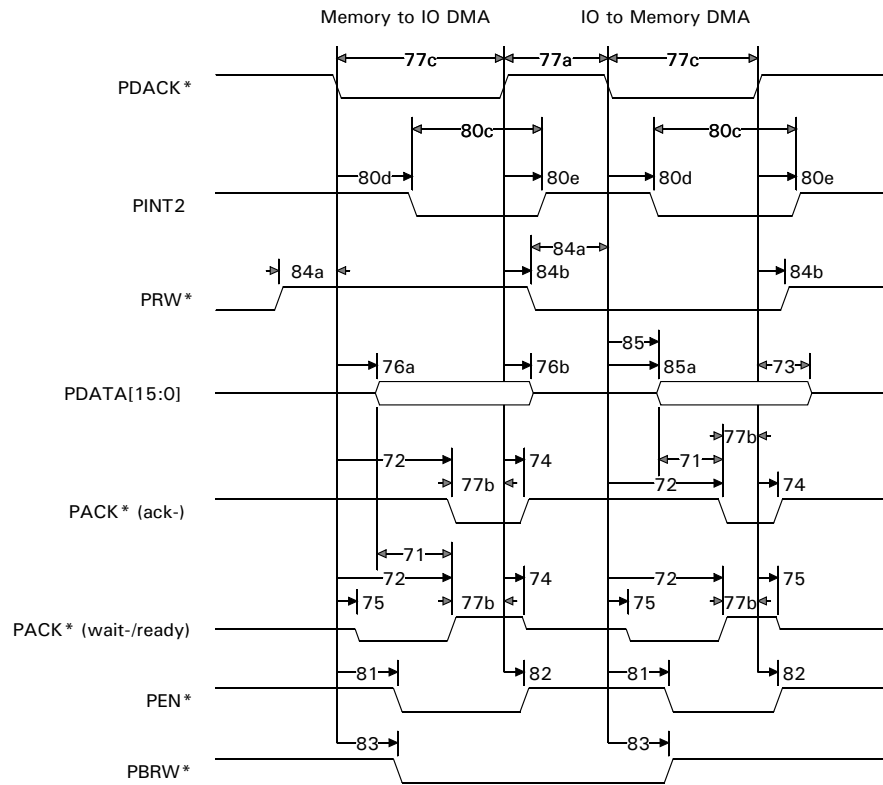
| Num | Characteristic                            | Note | Min           | Max                                  |
|-----|-------------------------------------------|------|---------------|--------------------------------------|
| 70a | PCS*/PDACK* low to PRW* sampled           | 1    |               | $T_{SYS} - 2.5$                      |
| 70b | PCS*/PDACK* low to PRW* hold time         | 1    | $4 * T_{SYS}$ |                                      |
| 71  | Read Data Valid to PACK* valid            |      | $T_{SYS}$     |                                      |
| 72  | PCS*/PDACK* low to PACK* low              | 3    | $T_{SYS}$     | $6 * T_{SYS}$                        |
| 72a | PCS* low to PACK* low                     | 4    | $7 * T_{SYS}$ | Determined by shared RAM access time |
| 72b | PCS*/PACK* low to PACK* low               | 5    | $2 * T_{SYS}$ | $4 * T_{SYS}$                        |
| 72c | PCS* low to PACK* valid (shared RAM only) | 6    | $7 * T_{SYS}$ | Determined by shared RAM access time |
| 73  | PCS*/PDACK* high to PDATA high impedance  |      | 0             | 7.84                                 |
| 74  | PCS*/PDACK* high to PACK* high            |      | 0             | 13                                   |
| 75  | PCS*/PDACK* low to PACK* (wait-) low      |      | 0             | 14                                   |
| 76a | PCS*/PDACK* low to Write Data valid       |      |               | $2 * T_{SYS}$                        |
| 76b | PCS*/PDACK* high to Write Data hold time  |      | 0             |                                      |
| 77a | PCS*/PDACK* width high (recovery)         |      | 16            |                                      |
| 77b | PACK* low to PCS*/PDACK* high (hold)      | 8    | 0             |                                      |
| 77c | PDACK* minimum low                        |      | 120           |                                      |
| 78a | Address valid to PCS* low                 |      | 0             |                                      |
| 78b | PCS* high to Address hold time            |      | 0             |                                      |
| 79  | PCS* low to PINT1/2 change (write)        |      | $3 * T_{SYS}$ | $5 * T_{SYS}$                        |
| 80a | PDACK* low to PDRQI*, PDRQO* high         |      |               | $5 * T_{SYS}$                        |
| 80b | PDRQO* high width                         |      | $5 * T_{SYS}$ |                                      |
| 80c | PDRQI* high width                         |      | $4 * T_{SYS}$ |                                      |
| 80d | PDACK* low to PINT2 low                   |      |               | 14                                   |
| 80e | PDACK* high to PINT2 high                 |      | 15            |                                      |
| 81  | PCS*/PDACK* low to PEN* low               | 2    | $1 * T_{SYS}$ | $3 * T_{SYS}$                        |
| 82  | PCS*/PDACK* high to PEN* high             | 2    | 0             | 13                                   |
| 83  | PCS*/PDACK* low to PBRW* low              | 2    | $1 * T_{SYS}$ | $2 * T_{SYS}$                        |
| 84a | PRW* valid to PDACK* low (setup)          | 1    | 0             |                                      |
| 84b | PDACK* high to PRW* hold time             | 1    | 0             |                                      |
| 85  | PDACK* low to PDATA valid                 | 7    | $3 * T_{SYS}$ | $5 * T_{SYS}$                        |
| 85a | PDACK* low to PDATA valid                 | 7    | $1 * T_{SYS}$ | $2 * T_{SYS}$                        |

**Notes:**

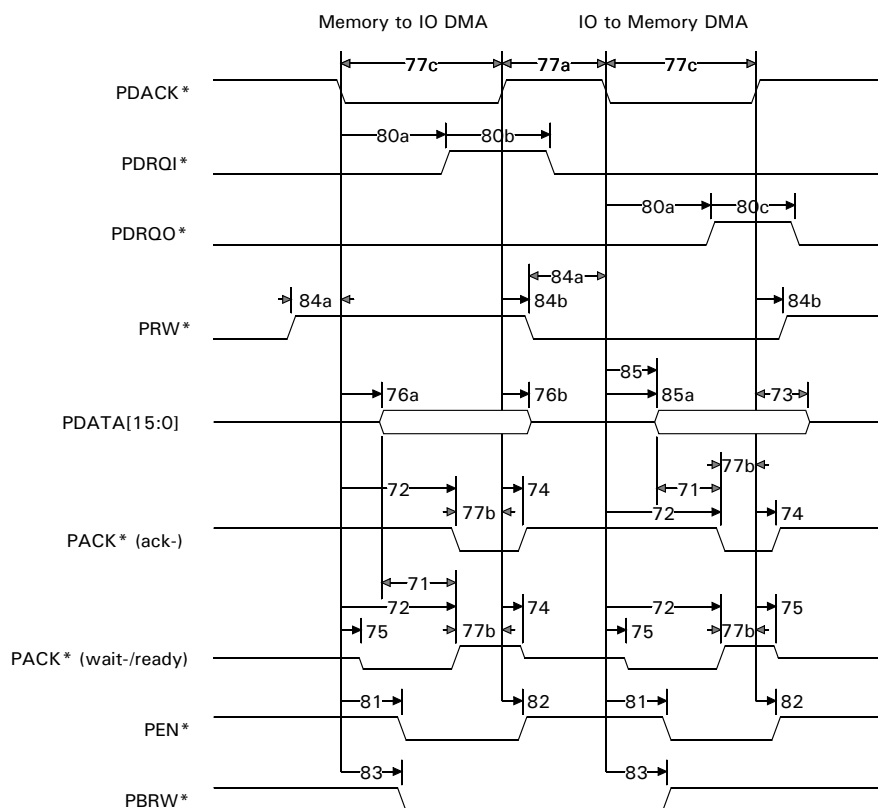
- Parameters 70a and 70b apply only when the ENI FAST bit is set to 0. When ENI FAST is set to 1, parameters 84a and 84b apply.
- The  $PEN^*$  and  $PBRW^*$  signals control an external bi-directional data bus transceiver for the PDATA bus that can drive only 2 mA.
- Parameter 72 applies only to ENI registers when FAST is set to 0. This does *not* apply to shared RAM access.
- Parameter 72a applies to all shared RAM accesses when FAST is set to 0. The max specification for  $PCS^*$  to  $PACK^*$  valid is larger for shared RAM accesses. The additional delay depends on the speed of the external RAM assigned to provide the physical shared RAM. Consequently, the maximum specification for shared RAM accesses is system-dependent.
- Parameter 72b applies to ENI register accesses when FAST is set to 1.
- Parameter 72c applies to ENI shared RAM accesses when FAST is set to 1.
- Parameter 85 applies when FAST is set to 0. Parameter 85a applies when FAST is set to 1.
- Parameter 77c can be reduced to  $3 \cdot T_{SYS}$  when FAST is set to 1.

**ENI Shared RAM and Register Cycle timing**

### ENI Single Direction DMA timing



# **ENI Dual Direction DMA timing**



P/N: 91001374\_B (formerly 8820002A)

Release date: March 2006

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