



DATA SHEET

BIPOLAR ANALOG INTEGRATED CIRCUIT μ PC8172TB

SILICON MMIC 2.5 GHz FREQUENCY UP-CONVERTER FOR WIRELESS TRANSCEIVER

DESCRIPTION

The μ PC8172TB is a silicon monolithic integrated circuit designed as frequency up-converter for wireless transceiver transmitter stage.

This IC is as same circuit current as conventional μ PC8106TB, but operates at higher frequency, higher gain and lower distortion. Consequently this IC is suitable for mobile communications.

FEATURES

- Recommended operating frequency : $f_{RFout} = 0.8$ to 2.5 GHz
- Higher IP_3 : $CG = 9.5$ dB TYP., $OIP_3 = +7.5$ dBm TYP. @ $f_{RFout} = 0.9$ GHz
- High-density surface mounting : 6-pin super minimold package
- Supply voltage : $V_{CC} = 2.7$ to 3.3 V

APPLICATIONS

- PCS1900M
- 2.4 GHz band transmitter/receiver system (wireless LAN etc.)

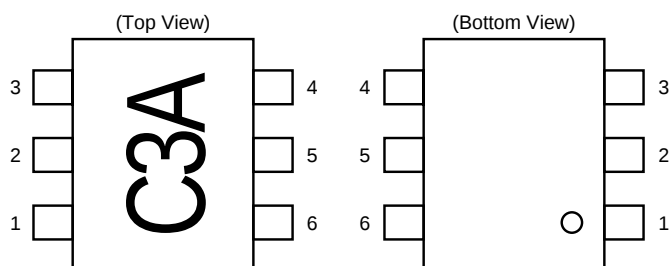
ORDERING INFORMATION

Part Number	Package	Marking	Supplying Form
μ PC8172TB-E3	6-pin super minimold	C3A	- Embossed tape 8 mm wide. - Pin 1, 2, 3 face the tape perforation side. - Qty 3 kpcs/reel.

Remark To order evaluation samples, please contact your nearby sales office.
(Part number for sample order: μ PC8172TB-A)

Caution Electro-static sensitive devices

PIN CONNECTIONS



Pin No.	Pin Name
1	IFinput
2	GND
3	LOinput
4	PS
5	V _{CC}
6	RFoutput

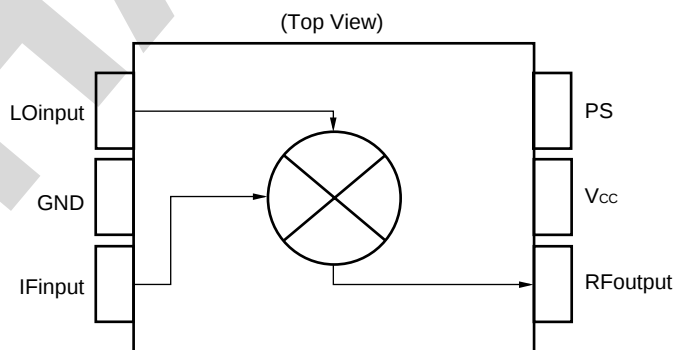
SERIES PRODUCTS ($T_A = +25^\circ\text{C}$, $V_{CC} = V_{RFout} = 3.0\text{ V}$, $Z_S = Z_L = 50\ \Omega$)

Part Number	I _{CC} (mA)	f _{RFout} (GHz)	CG (dB)		
			@RF 0.9 GHz ^{Note}	@RF 1.9 GHz	@RF 2.4 GHz
μ PC8172TB	9	0.8 to 2.5	9.5	8.5	8.0
μ PC8106TB	9	0.4 to 2.0	9	7	–
μ PC8109TB	5	0.4 to 2.0	6	4	–
μ PC8163TB	16.5	0.8 to 2.0	9	5.5	–

Part Number	P _{O(sat)} (dBm)			OIP ₃ (dBm)		
	@RF 0.9 GHz ^{Note}	@RF 1.9 GHz	@RF 2.4 GHz	@RF 0.9 GHz ^{Note}	@RF 1.9 GHz	@RF 2.4 GHz
μ PC8172TB	+0.5	0	–0.5	+7.5	+6.0	+4.0
μ PC8106TB	–2	–4	–	+5.5	+2.0	–
μ PC8109TB	–5.5	–7.5	–	+1.5	–1.0	–
μ PC8163TB	+0.5	–2	–	+9.5	+6.0	–

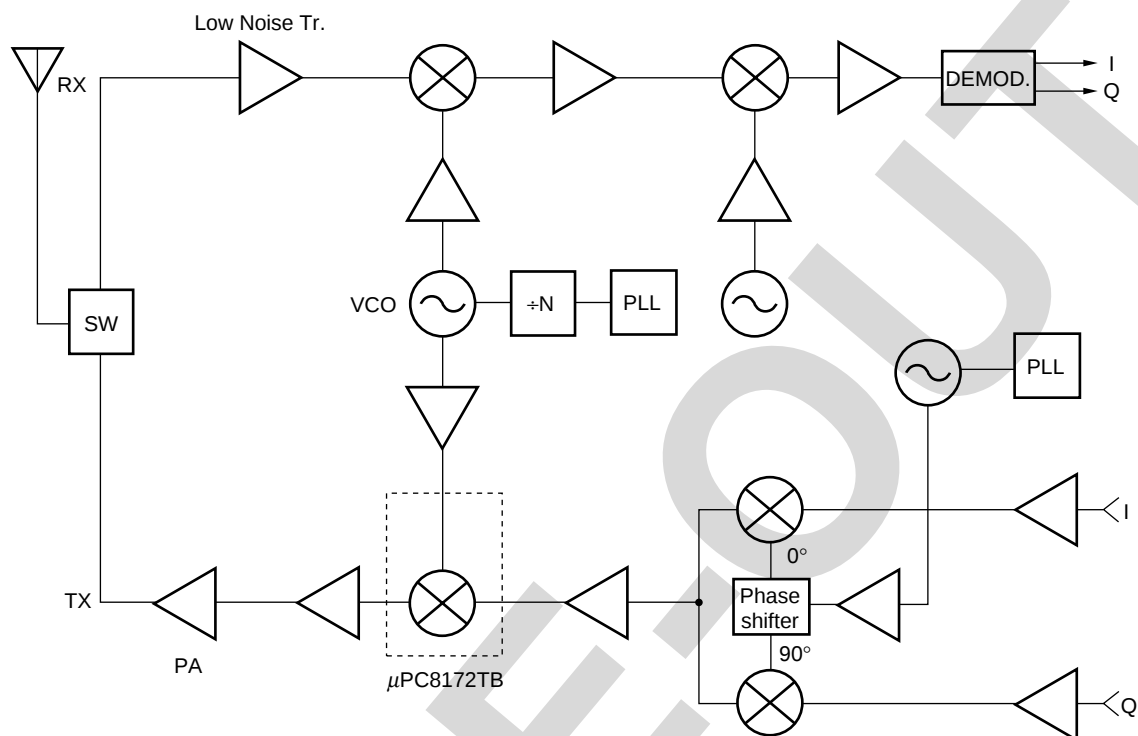
Note f_{RFout} = 0.83 GHz @ μ PC8163TB

Remark Typical performance. Please refer to **ELECTRICAL CHARACTERISTICS** in detail.
To know the associated product, please refer to each latest data sheet.

BLOCK DIAGRAM (FOR THE μ PC8172TB)

SYSTEM APPLICATION EXAMPLES (SCHEMATICS OF IC LOCATION IN THE SYSTEM)

Wireless Transceiver

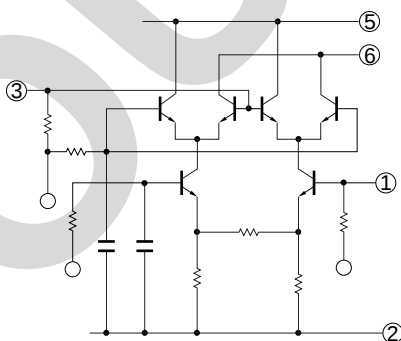
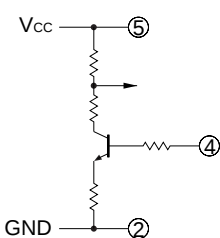


To know the associated products, please refer to each latest data sheet.

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1. PIN EXPLANATION

Pin No.	Pin Name	Applied Voltage (V)	Pin Voltage (V) ^{Note}	Function and Explanation	Equivalent Circuit						
1	IFinput	–	1.4	This pin is IF input to double balanced mixer (DBM). The input is designed as high impedance. The circuit contributes to suppress spurious signal. Also this symmetrical circuit can keep specified performance insensitive to process-condition distribution. For above reason, double balanced mixer is adopted.							
2	GND	GND	–	GND pin. Ground pattern on the board should be formed as wide as possible. Track Length should be kept as short as possible to minimize ground impedance.							
3	LOinput	–	2.3	Local input pin. Recommendable input level is –10 to 0 dBm.							
5	Vcc	2.7 to 3.3	–	Supply voltage pin.							
6	RFoutput	Same bias as Vcc through external inductor	–	This pin is RF output from DBM. This pin is designed as open collector. Due to the high impedance output, this pin should be externally equipped with LC matching circuit to next stage.							
4	PS	Vcc/GND	–	Power save control pin. Bias controls operation as follows. <table border="1" data-bbox="686 1260 1006 1400"><thead><tr><th>Pin bias</th><th>Control</th></tr></thead><tbody><tr><td>Vcc</td><td>Operation</td></tr><tr><td>GND</td><td>Power Save</td></tr></tbody></table>	Pin bias	Control	Vcc	Operation	GND	Power Save	
Pin bias	Control										
Vcc	Operation										
GND	Power Save										

Note Each pin voltage is measured with $V_{CC} = V_{PS} = V_{RFout} = 3.0$ V.

★ 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Rating	Unit
Supply Voltage	V_{CC}	$T_A = +25^\circ\text{C}$	3.6	V
PS pin Input Voltage	V_{PS}	$T_A = +25^\circ\text{C}$	3.6	V
Power Dissipation of Package	P_D	Mounted on double-side copperclad $50 \times 50 \times 1.6$ mm epoxy glass PWB ($T_A = +85^\circ\text{C}$)	270	mW
Operating Ambient Temperature	T_A		-40 to +85	$^\circ\text{C}$
Storage Temperature	T_{stg}		-55 to +150	$^\circ\text{C}$
Input Power	P_{in}		+10	dBm

3. RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}	The same voltage should be applied to pin 5 and 6	2.7	3.0	3.3	V
Operating Ambient Temperature	T_A		-40	+25	+85	$^\circ\text{C}$
Local Input Level	P_{LOin}	$Z_s = 50 \Omega$ (without matching)	-10	-5	0	dBm
RF Output Frequency	f_{RFout}	With external matching circuit	0.8	–	2.5	GHz
IF Input Frequency	f_{IFin}		50	–	400	MHz

4. ELECTRICAL CHARACTERISTICS

($T_A = +25^\circ\text{C}$, $V_{CC} = V_{RFout} = 3.0 \text{ V}$, $f_{IFin} = 240 \text{ MHz}$, $P_{LOin} = -5 \text{ dBm}$, and $V_{PS} \geq 2.7 \text{ V}$ unless otherwise specified)

Parameter	Symbol	Test Conditions ^{Note}	MIN.	TYP.	MAX.	Unit
Circuit Current	I_{CC}	No Signal	5.5	9.0	13	mA
Circuit Current In Power Save Mode	$I_{CC(PS)}$	$V_{PS} = 0 \text{ V}$	–	–	2	μA
Conversion Gain	CG1	$f_{RFout} = 0.9 \text{ GHz}$, $P_{IFin} = -30 \text{ dBm}$	6.5	9.5	12.5	dB
	CG2	$f_{RFout} = 1.9 \text{ GHz}$, $P_{IFin} = -30 \text{ dBm}$	5.5	8.5	11.5	dB
	CG3	$f_{RFout} = 2.4 \text{ GHz}$, $P_{IFin} = -30 \text{ dBm}$	5	8.0	11.0	dB
Saturated RF Output Power	$P_{O(sat)1}$	$f_{RFout} = 0.9 \text{ GHz}$, $P_{IFin} = 0 \text{ dBm}$	-2.5	+0.5	–	dBm
	$P_{O(sat)2}$	$f_{RFout} = 1.9 \text{ GHz}$, $P_{IFin} = 0 \text{ dBm}$	-3.5	0	–	dBm
	$P_{O(sat)3}$	$f_{RFout} = 2.4 \text{ GHz}$, $P_{IFin} = 0 \text{ dBm}$	-4	-0.5	–	dBm

Note $f_{RFout} < f_{LOin}$ @ $f_{RFout} = 0.9 \text{ GHz}$

$f_{LOin} < f_{RFout}$ @ $f_{RFout} = 1.9 \text{ GHz}/2.4 \text{ GHz}$

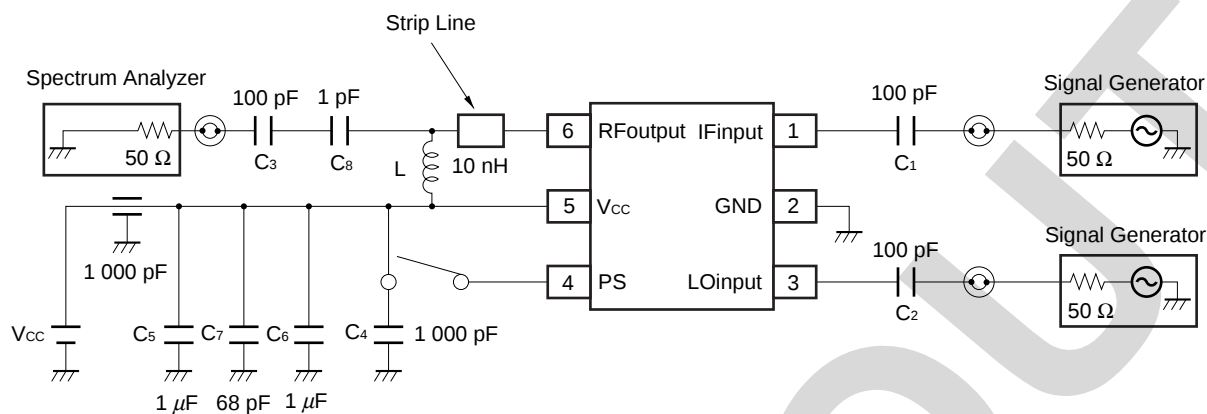
5. OTHER CHARACTERISTICS, FOR REFERENCE PURPOSES ONLY(T_A = +25°C, V_{CC} = V_{RFout} = 3.0 V, P_{LOin} = -5 dBm, and V_{PS} ≥ 2.7 V unless otherwise specified)

Parameter		Symbol	Test Conditions ^{Note}		Data	Unit
Output Third-Order Distortion Intercept Point		OIP ₃₁	f _{RFout} = 0.9 GHz	f _{iFin1} = 240 MHz f _{iFin2} = 241 MHz	+7.5	dBm
		OIP ₃₂	f _{RFout} = 1.9 GHz		+6.0	dBm
		OIP ₃₃	f _{RFout} = 2.4 GHz		+4.0	dBm
Input Third-Order Distortion Intercept Point		IIP ₃₁	f _{RFout} = 0.9 GHz	f _{iFin1} = 240 MHz f _{iFin2} = 241 MHz	−2.0	dBm
		IIP ₃₂	f _{RFout} = 1.9 GHz		−2.5	dBm
		IIP ₃₃	f _{RFout} = 2.4 GHz		−4.0	dBm
SSB Noise Figure		SSB•NF1	f _{RFout} = 0.9 GHz, f _{iFin} = 240 MHz		9.5	dB
		SSB•NF2	f _{RFout} = 1.9 GHz, f _{iFin} = 240 MHz		10.4	dB
		SSB•NF3	f _{RFout} = 2.4 GHz, f _{iFin} = 240 MHz		10.6	dB
Power Save Response Time	Rise time	T _{PS(rise)}	V _{PS} : GND → V _{CC}		1	μs
	Fall time	T _{PS(fall)}	V _{PS} : V _{CC} → GND		1.5	μs

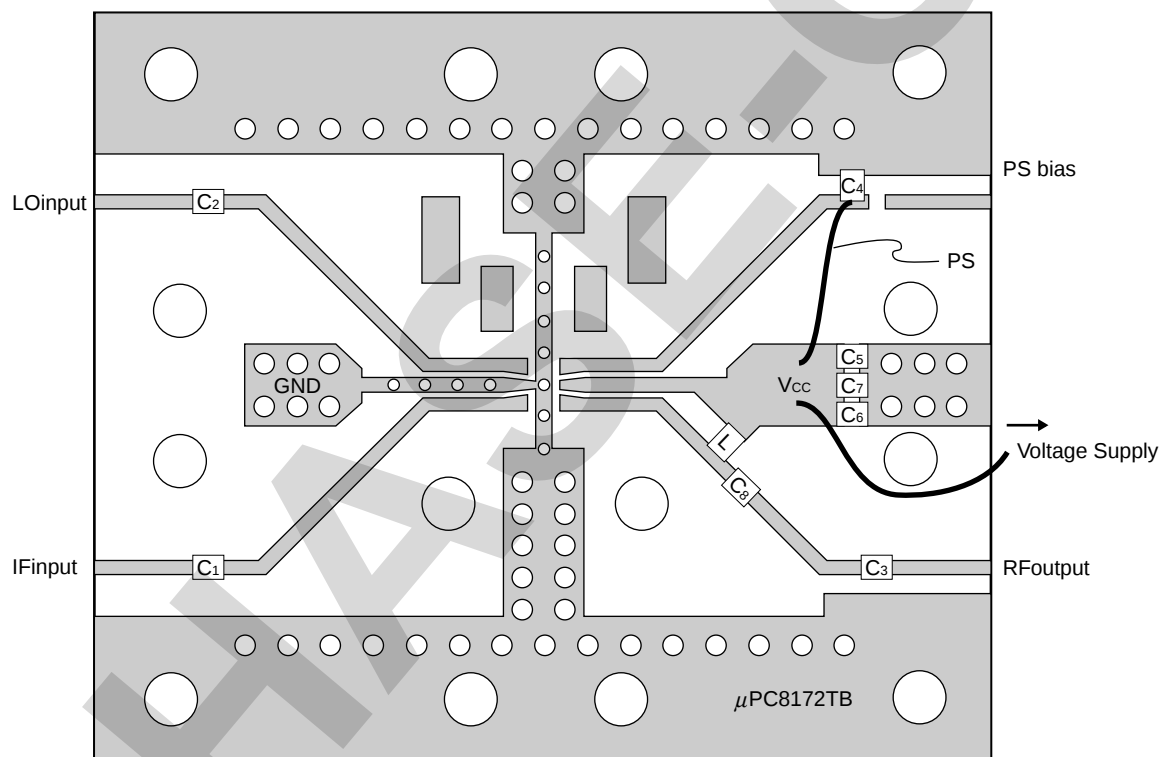
Note f_{RFout} < f_{LOin} @ f_{RFout} = 0.9 GHzf_{LOin} < f_{RFout} @ f_{RFout} = 1.9 GHz/2.4 GHz

6. TEST CIRCUIT

★ 6.1 TEST CIRCUIT 1 ($f_{RFout} = 900$ MHz)



EXAMPLE OF TEST CIRCUIT 1 ASSEMBLED ON EVALUATION BOARD



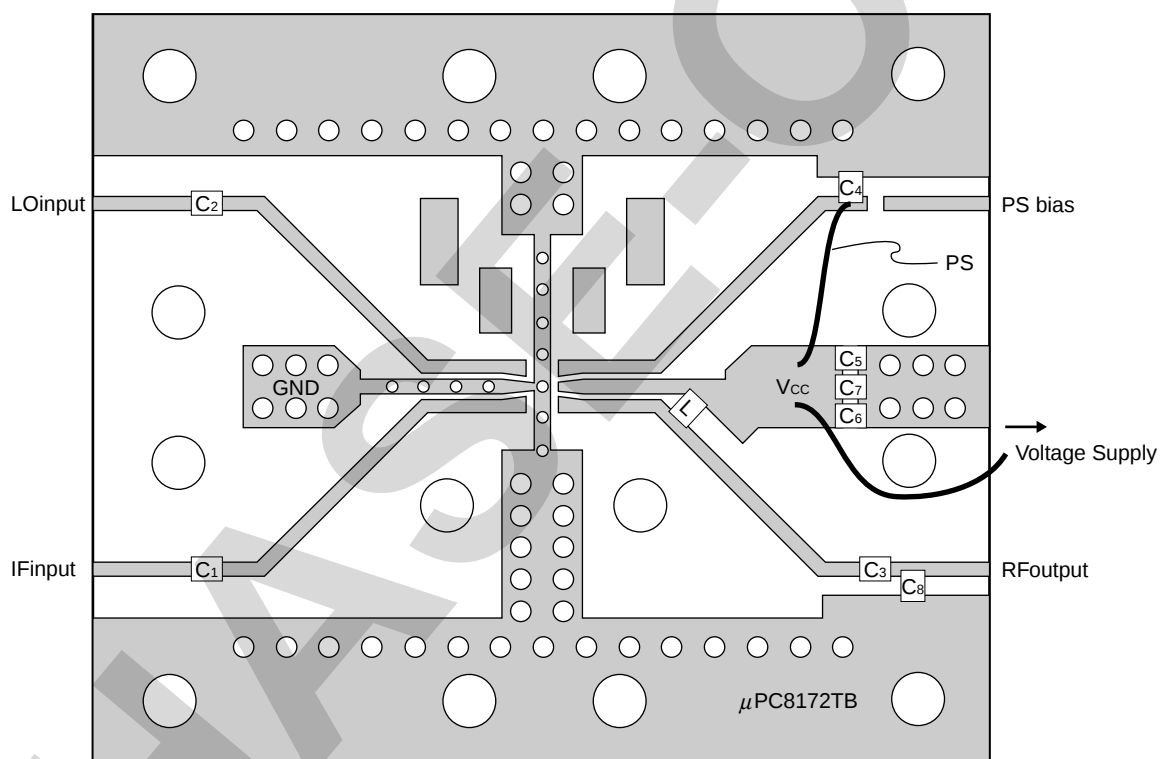
COMPONENT LIST

Form	Symbol	Value
Chip capacitor	C1, C2, C3	100 pF
	C4	1 000 pF
	C5, C6	1 μ F
	C7	68 pF
	C8	1 pF
Chip inductor	L	10 nH ^{Note}

- (*1) 35 × 42 × 0.4 mm polyimide board, double-sided copper clad
 (*2) Ground pattern on rear of the board
 (*3) Solder plated patterns
 (*4) ○○: Through holes

Note 10 nH: LL1608-FH10N (TOKO Co., Ltd.)

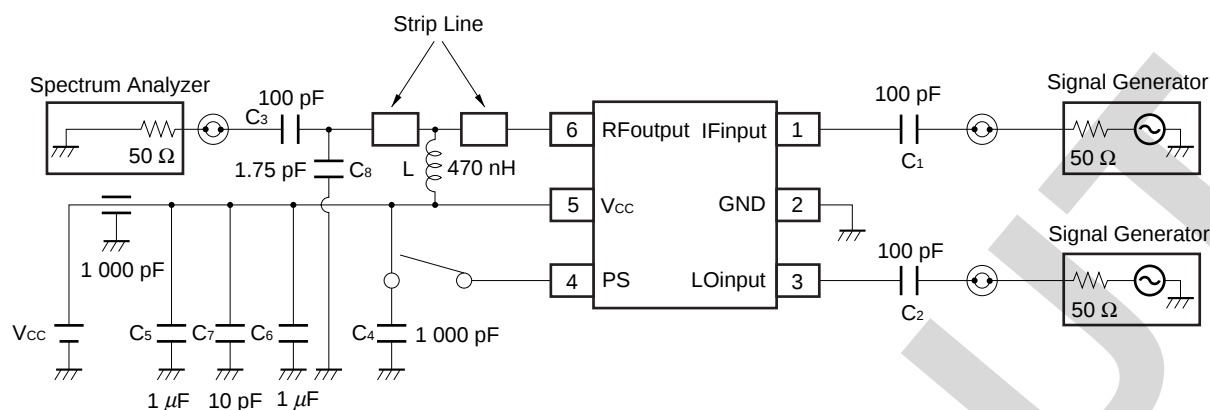
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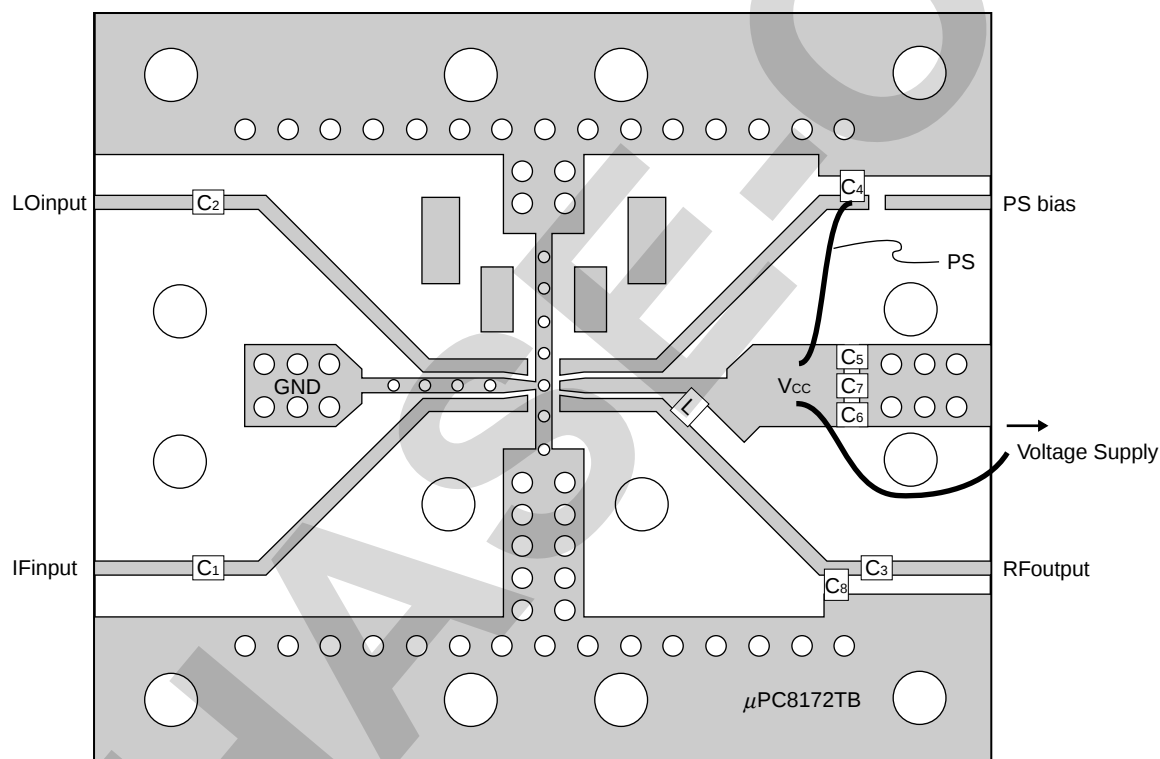
COMPONENT LIST

- (*1) 35 × 42 × 0.4 mm polyimide board, double-sided copper clad
- (*2) Ground pattern on rear of the board
- (*3) Solder plated patterns
- (*4) ○○○: Through holes

Note 470 nH: LL2012-FR47 (TOKO Co., Ltd.)

★ 6.3 TEST CIRCUIT 3 ($f_{RFout} = 2.4\text{ GHz}$)

EXAMPLE OF TEST CIRCUIT 3 ASSEMBLED ON EVALUATION BOARD



COMPONENT LIST

Form	Symbol	Value
Chip capacitor	C ₁ , C ₂ , C ₃	100 pF
	C ₄	1 000 pF
	C ₅ , C ₆	1 μF
	C ₇	10 pF
	C ₈	1.75 pF
	L	470 nH ^{Note}
Chip inductor	L	470 nH ^{Note}

(*1) 35 × 42 × 0.4 mm polyimide board, double-sided copper clad

(*2) Ground pattern on rear of the board

(*3) Solder plated patterns

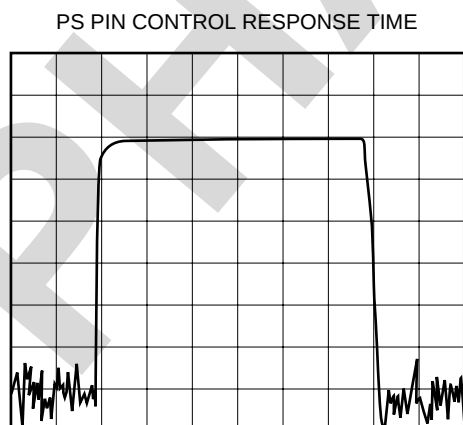
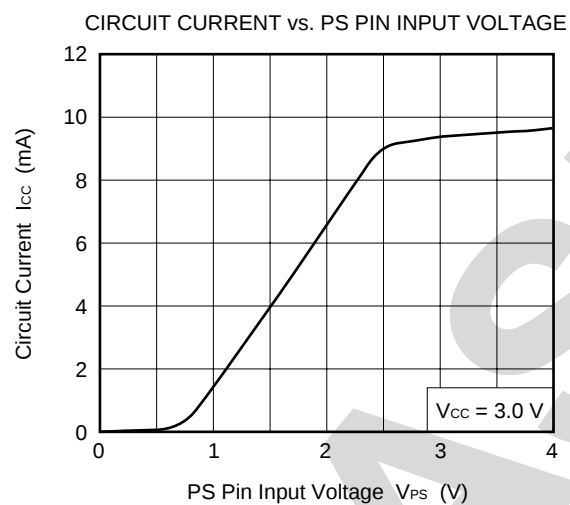
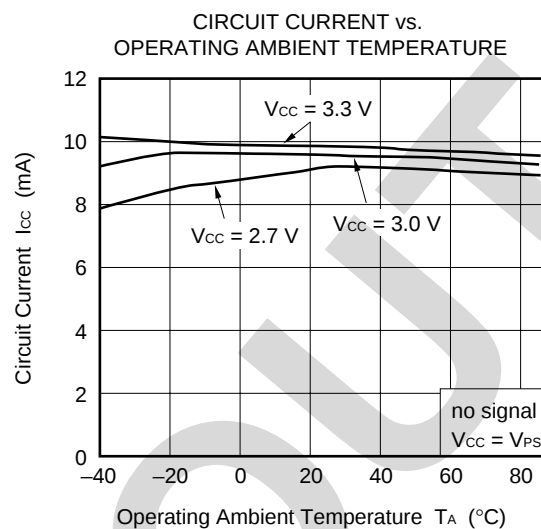
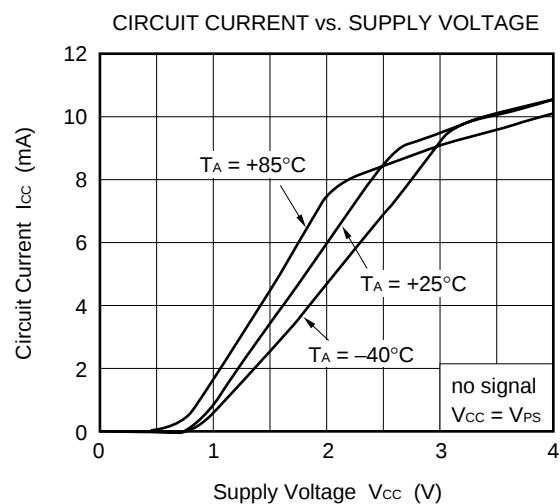
(*4) ○○: Through holes

Note 470 nH: LL2012-FR47 (TOKO Co., Ltd.)

Caution The test circuits and board pattern on data sheet are for performance evaluation use only (They are not recommended circuits). In the case of actual design-in, matching circuit should be determined using S-parameter of desired frequency in accordance to actual mounting pattern.

PHASE OUT

★ 7. TYPICAL CHARACTERISTICS (Unless otherwise specified, $T_A = +25^\circ\text{C}$, $V_{CC} = V_{RFout}$)



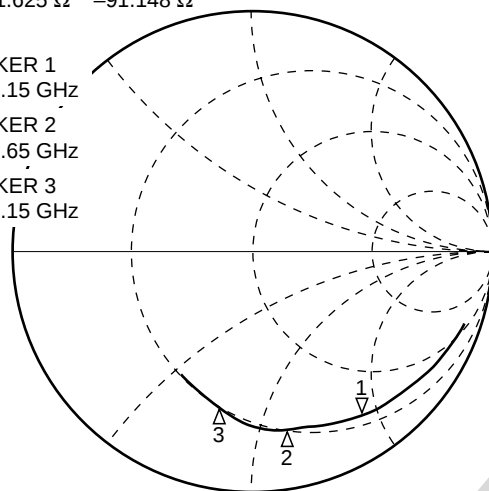
REF LVL = 0 dBm
 ATT = 10 dB
 10 dB/DIV (Vertical axis)
 CENTER = 0.9 GHz
 SPAN = 0 Hz
 RBW = 3 MHz
 VBW = 3 MHz
 SWP = 50 μsec
 5 μsec /DIV (Horizontal axis)

★ **S-PARAMETERS FOR EACH PORT** ($V_{CC} = V_{PS} = V_{RFout} = 3.0\text{ V}$)
 (The parameters are monitored at DUT pins)

LO port

S_{11} Z
 REF 1.0 Units
 1 200.0 mUnits/
 ∇ 21.625 Ω -91.148 Ω
 hp

MARKER 1
 1.15 GHz
 MARKER 2
 1.65 GHz
 MARKER 3
 2.15 GHz

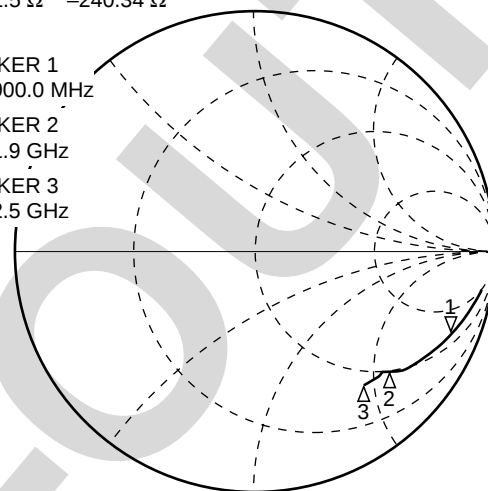


START 0.400000000 GHz
 STOP 2.500000000 GHz

RF port (without matching)

S_{22} Z
 REF 1.0 Units
 1 200.0 mUnits/
 ∇ 71.5 Ω -240.34 Ω
 hp

MARKER 1
 900.0 MHz
 MARKER 2
 1.9 GHz
 MARKER 3
 2.5 GHz

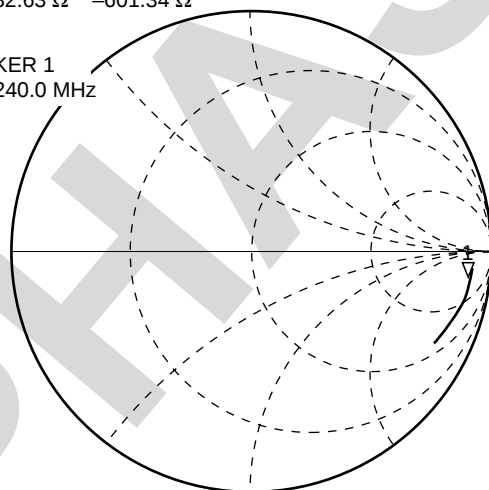


START 0.400000000 GHz
 STOP 2.500000000 GHz

IF port

S_{11} Z
 REF 1.0 Units
 1 200.0 mUnits/
 ∇ 332.63 Ω -601.34 Ω
 hp

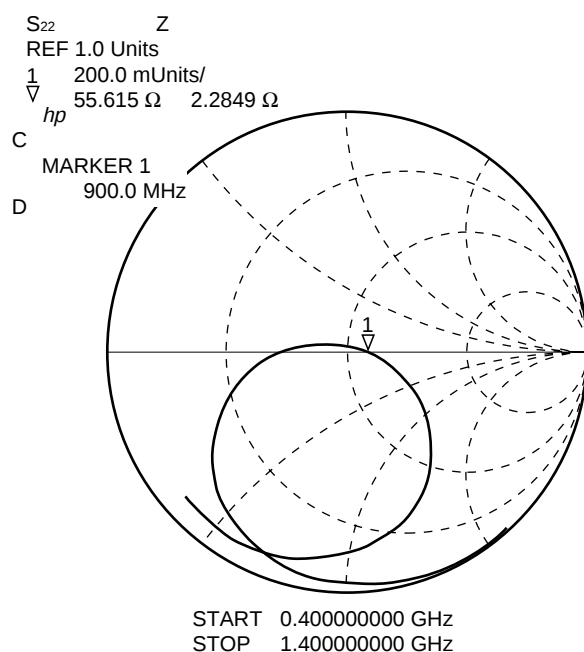
MARKER 1
 240.0 MHz



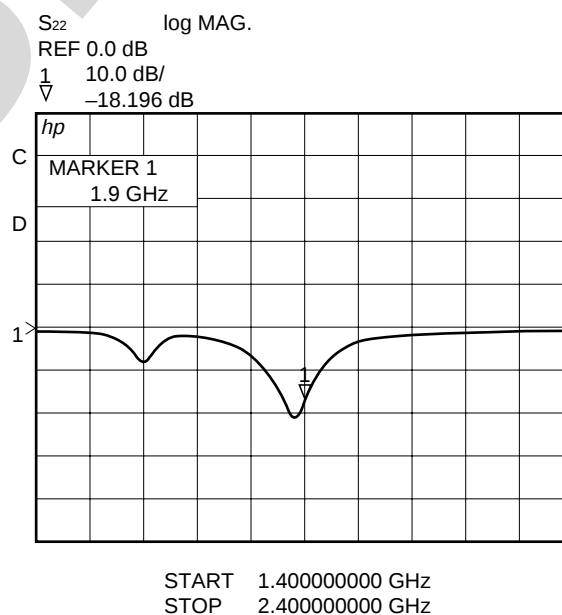
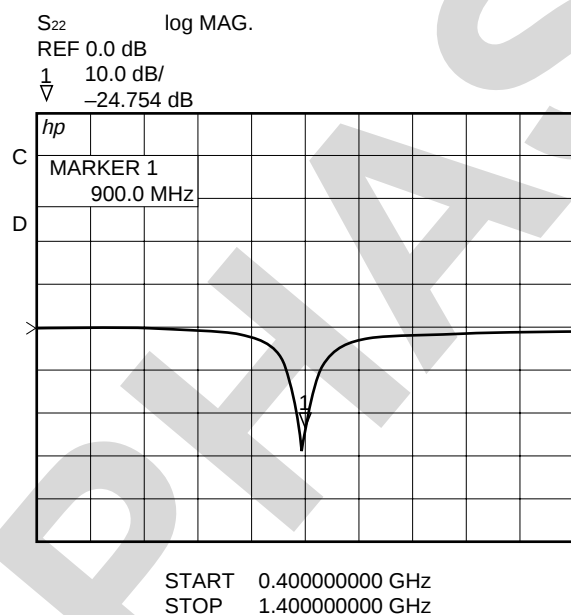
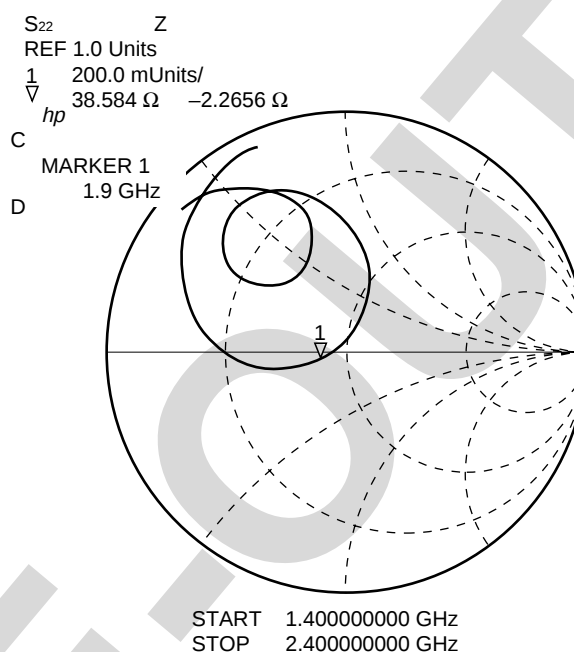
START 0.100000000 GHz
 STOP 1.000000000 GHz

★ **S-PARAMETERS FOR MATCHED RF OUTPUT** ($V_{CC} = V_{PS} = V_{RFout} = 3.0\text{ V}$) **—ON EVALUATION BOARD—**
(S22 data are monitored at RF connector on board)

900 MHz (matched in test circuit 1)

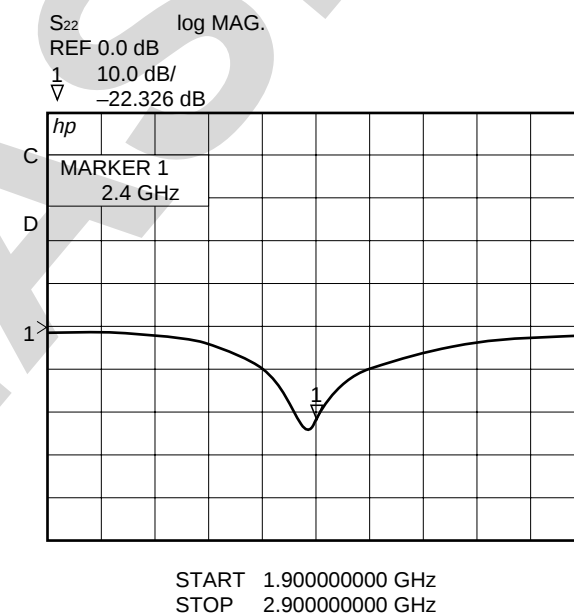
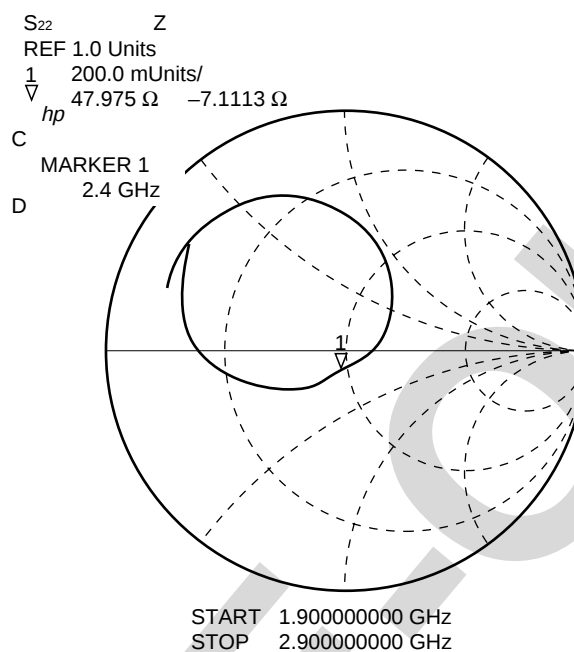


1.9 GHz (matched in test circuit 2)

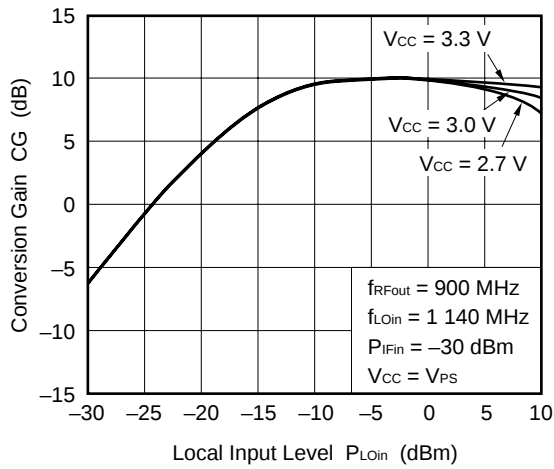


★ **S-PARAMETERS FOR MATCHED RF OUTPUT** ($V_{CC} = V_{PS} = V_{RFout} = 3.0\text{ V}$) **–ON EVALUATION BOARD–**
(S_{22} data are monitored at RF connector on board)

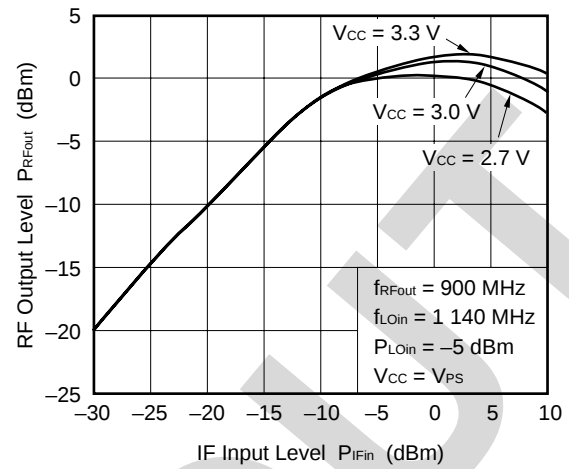
2.4 GHz (matched in test circuit 3)



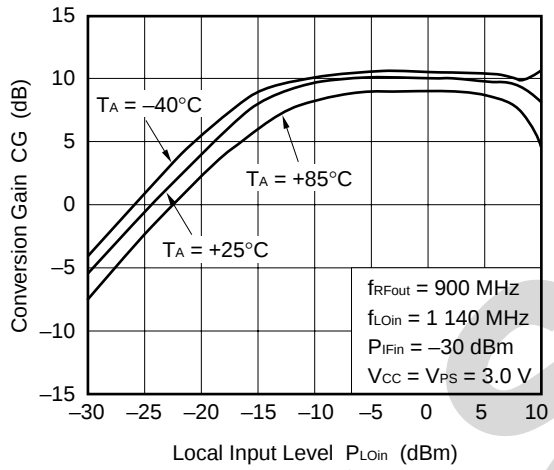
CONVERSION GAIN vs. LOCAL INPUT LEVEL



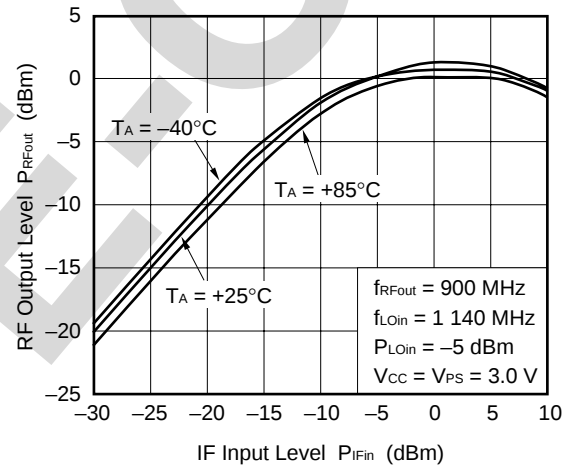
RF OUTPUT LEVEL vs. IF INPUT LEVEL

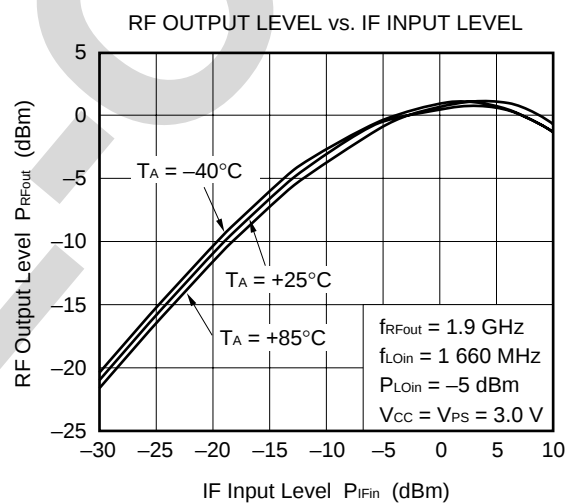
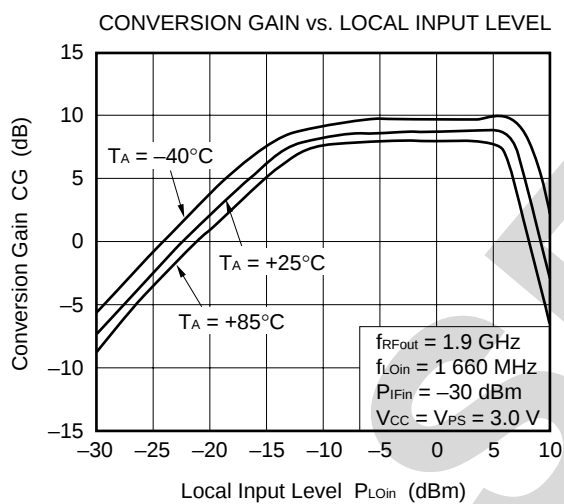
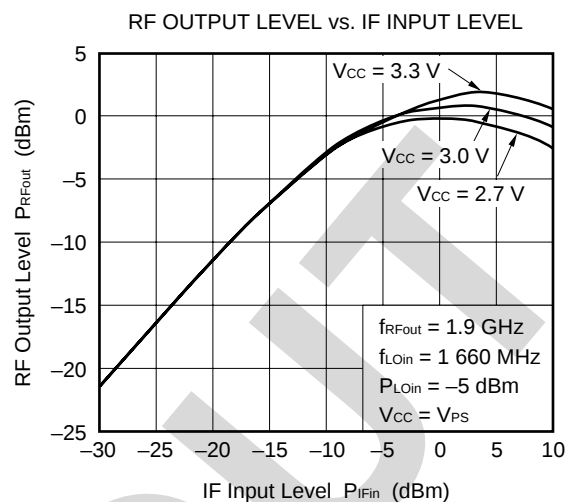
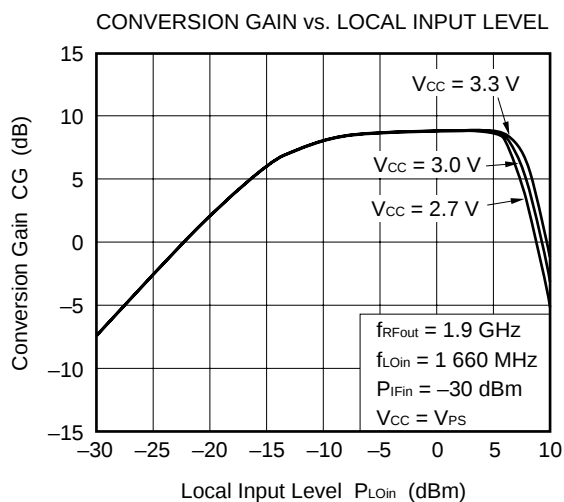


CONVERSION GAIN vs. LOCAL INPUT LEVEL

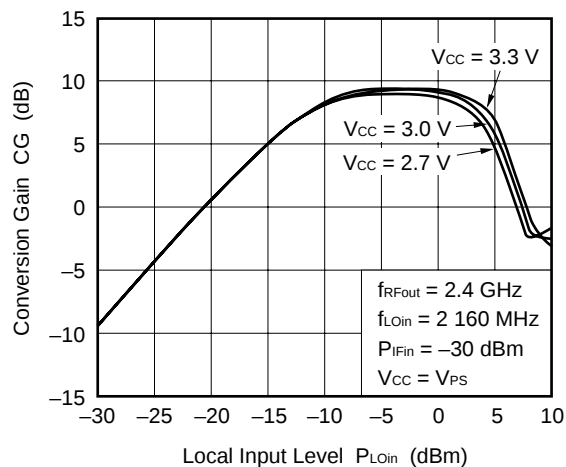


RF OUTPUT LEVEL vs. IF INPUT LEVEL

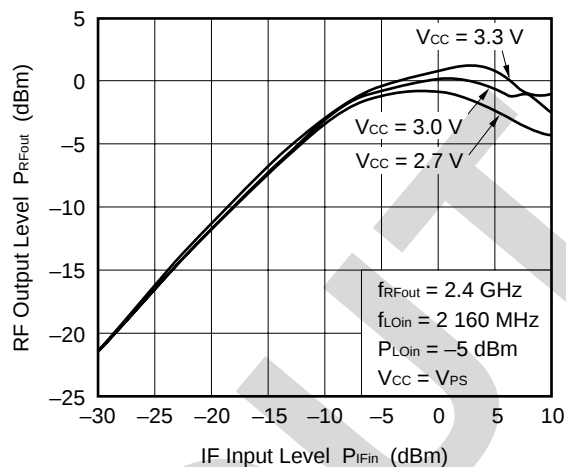




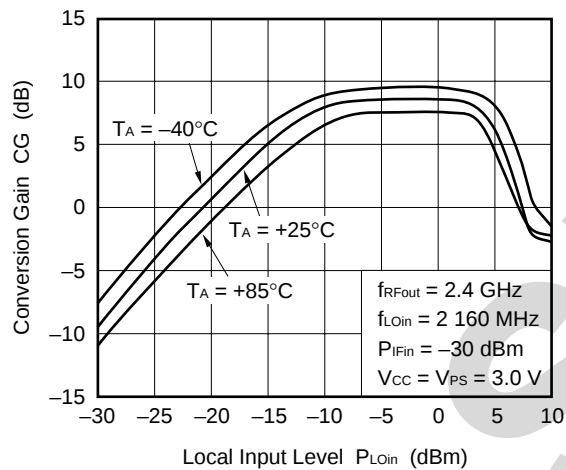
CONVERSION GAIN vs. LOCAL INPUT LEVEL



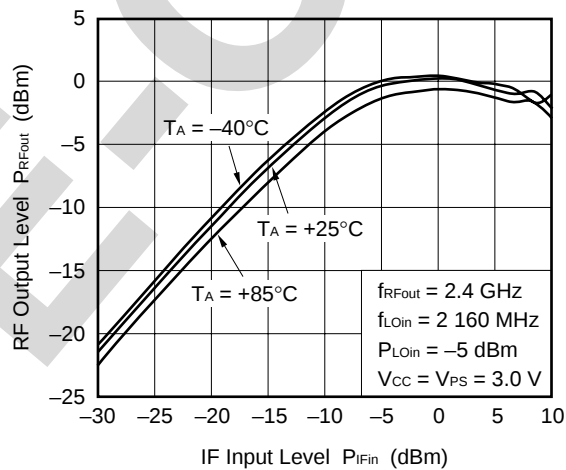
RF OUTPUT LEVEL vs. IF INPUT LEVEL

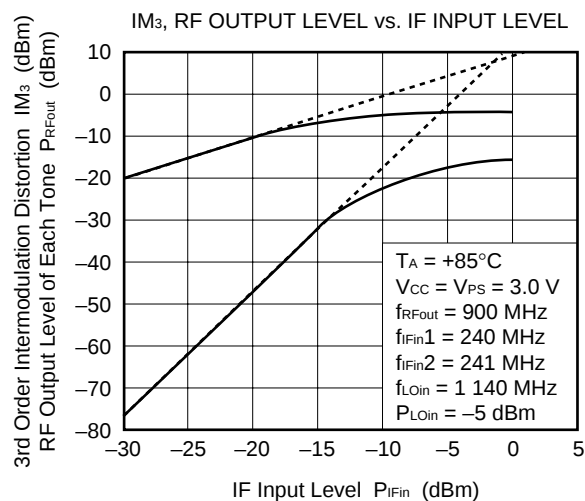
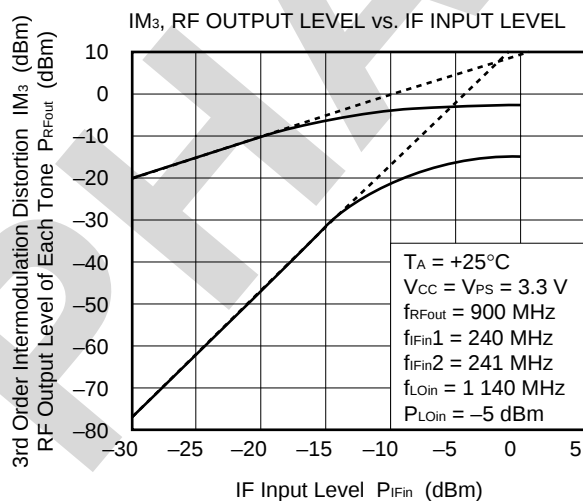
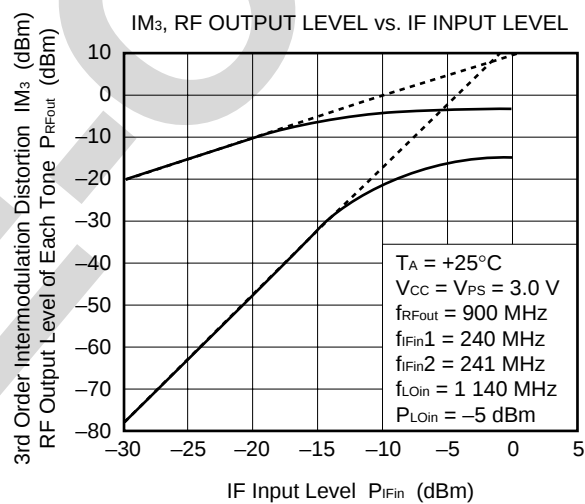
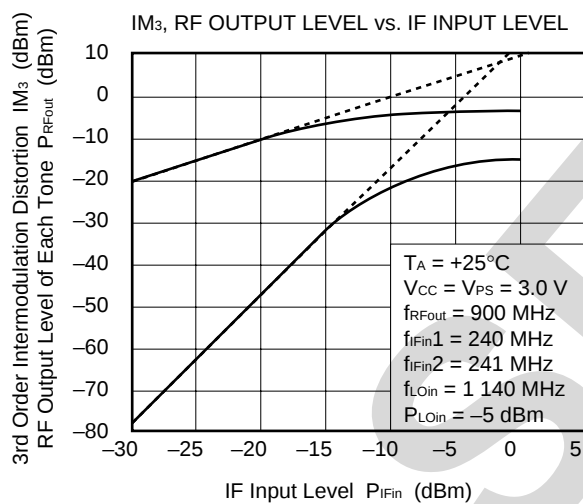
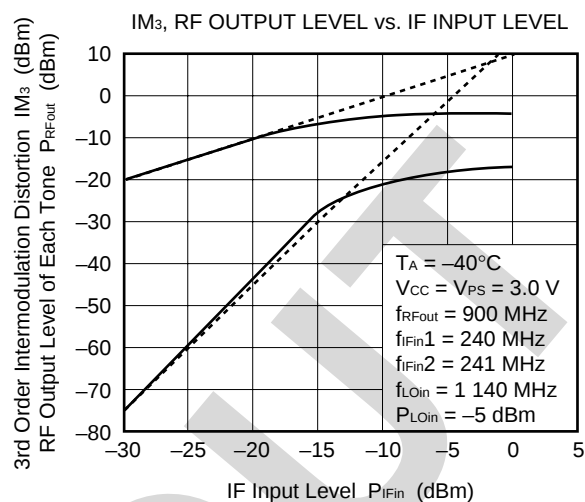
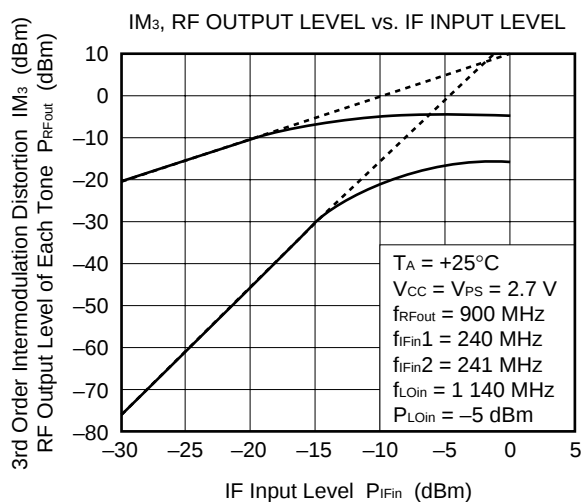


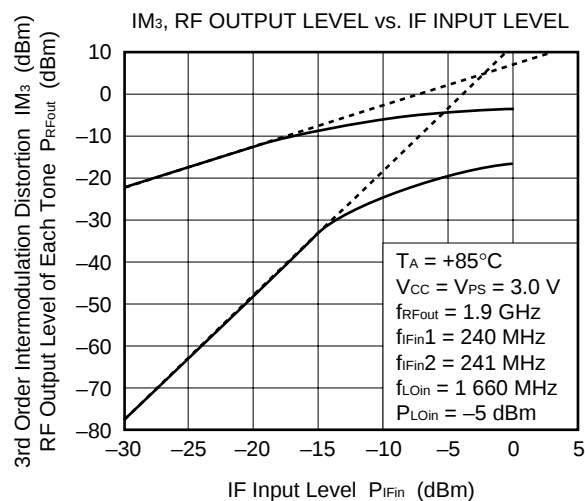
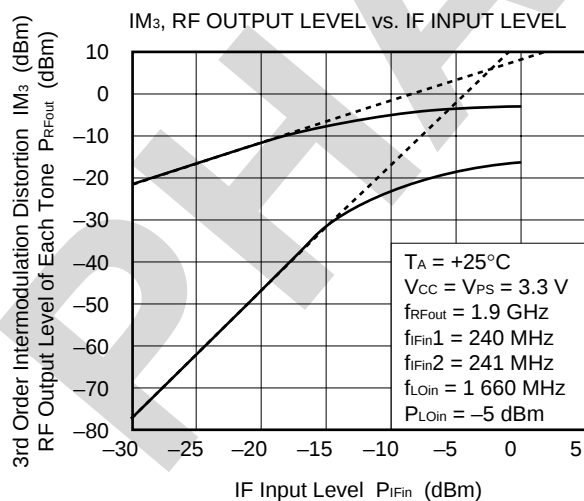
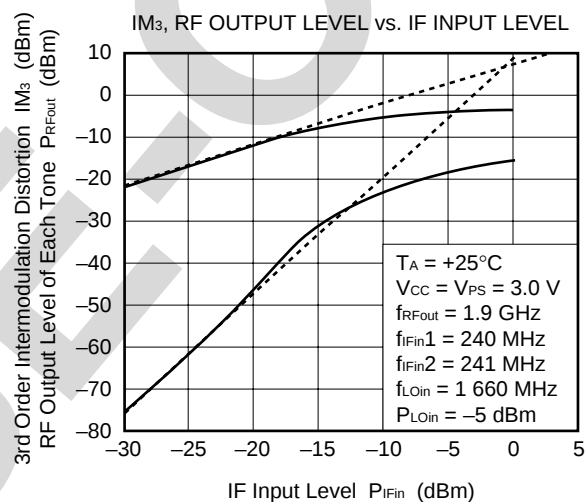
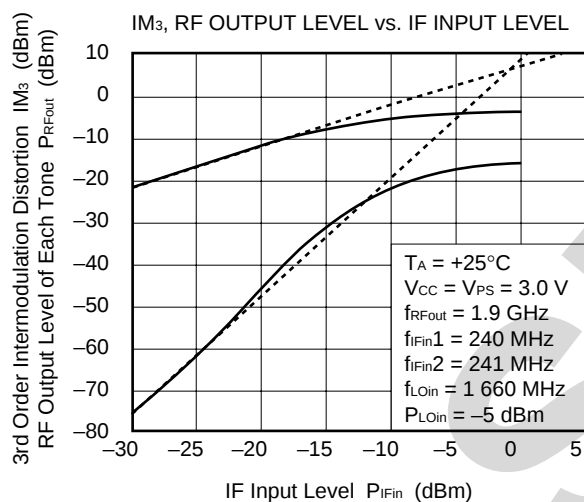
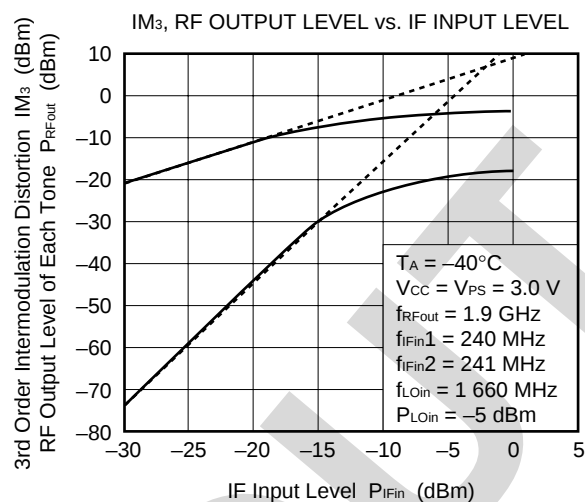
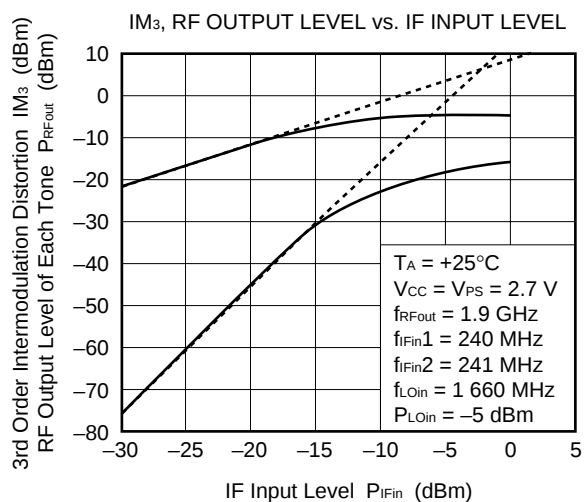
CONVERSION GAIN vs. LOCAL INPUT LEVEL

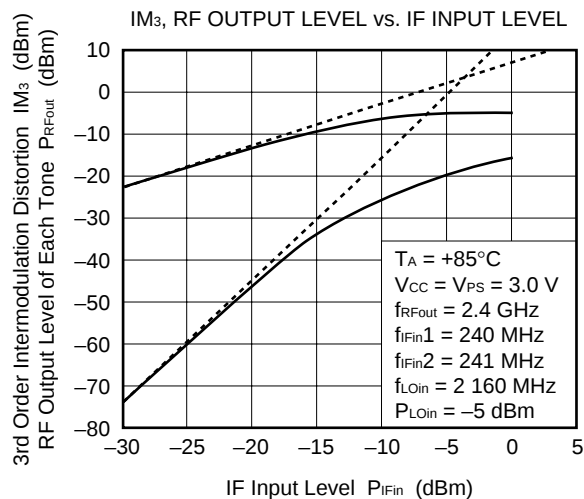
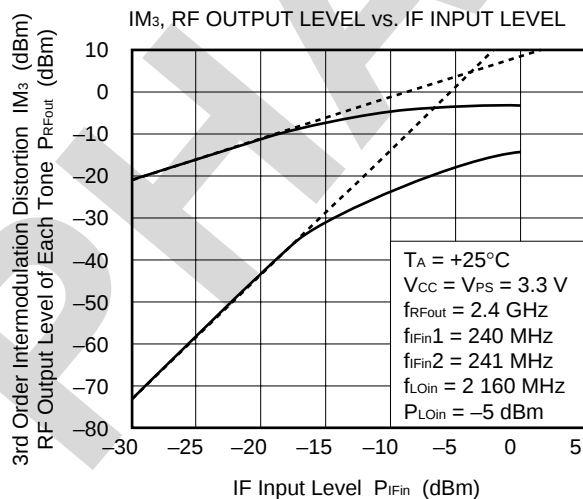
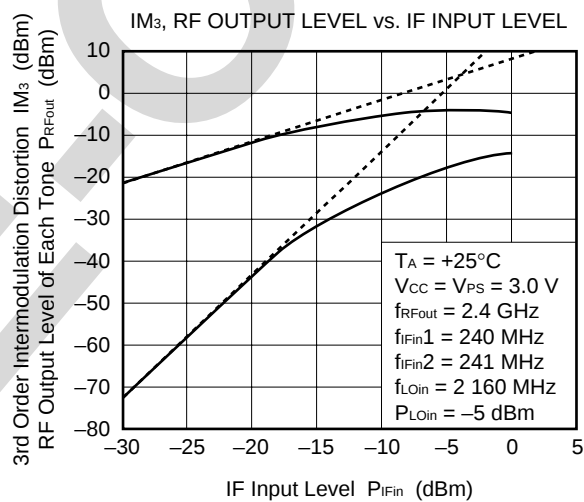
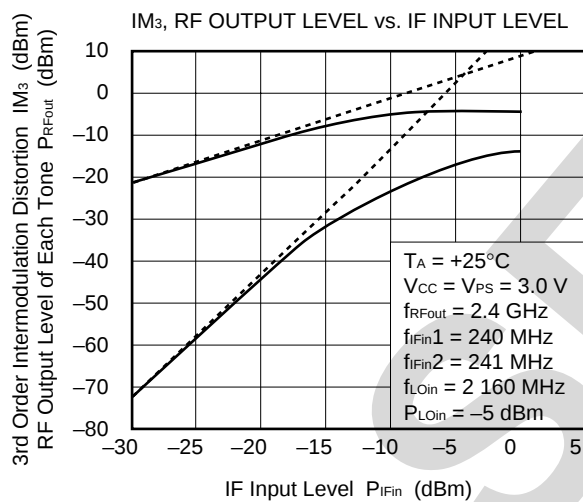
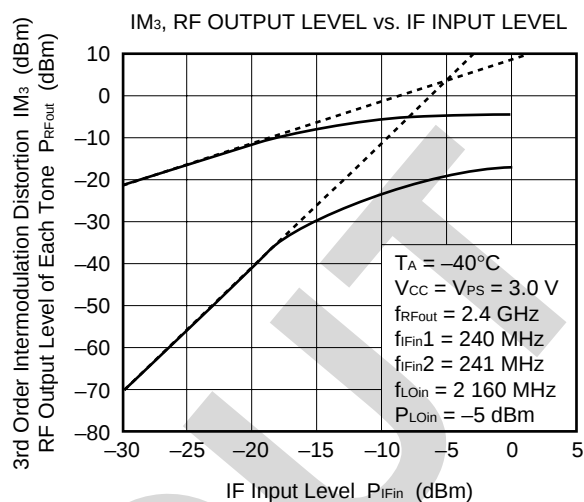
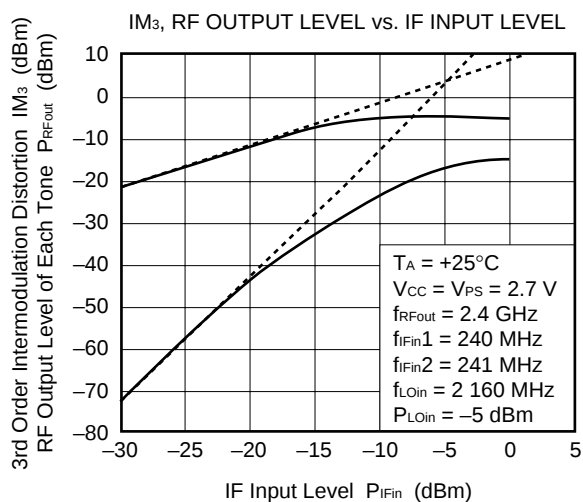


RF OUTPUT LEVEL vs. IF INPUT LEVEL

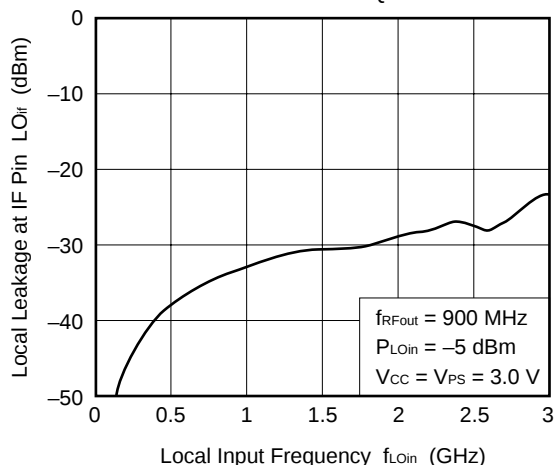




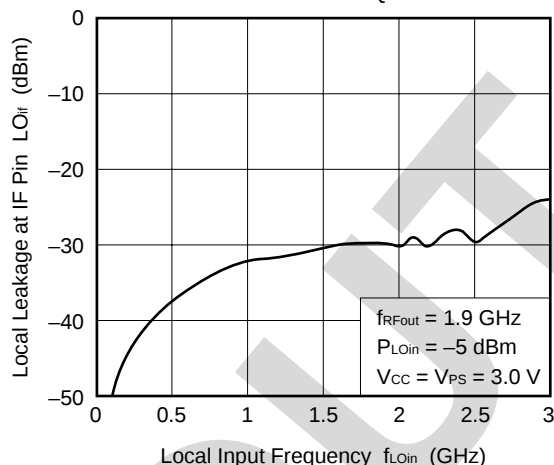




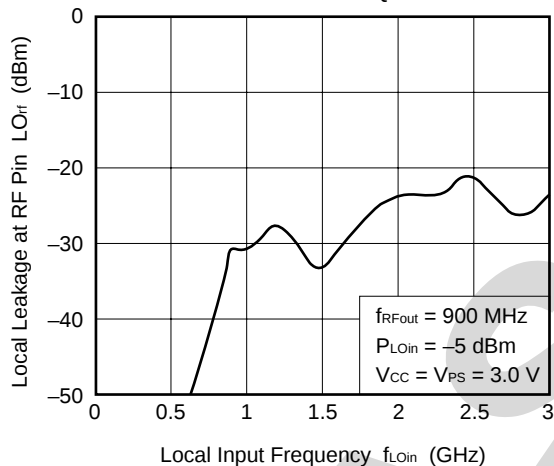
LOCAL LEAKAGE AT IF PIN vs.
LOCAL INPUT FREQUENCY



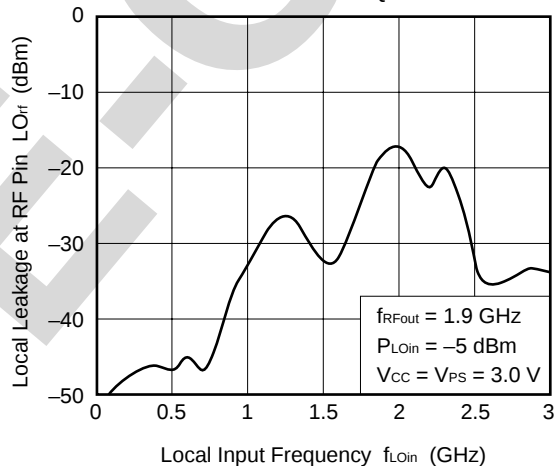
LOCAL LEAKAGE AT IF PIN vs.
LOCAL INPUT FREQUENCY



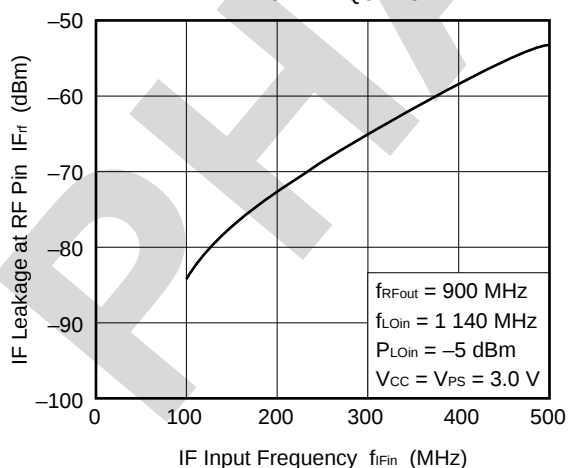
LOCAL LEAKAGE AT RF PIN vs.
LOCAL INPUT FREQUENCY



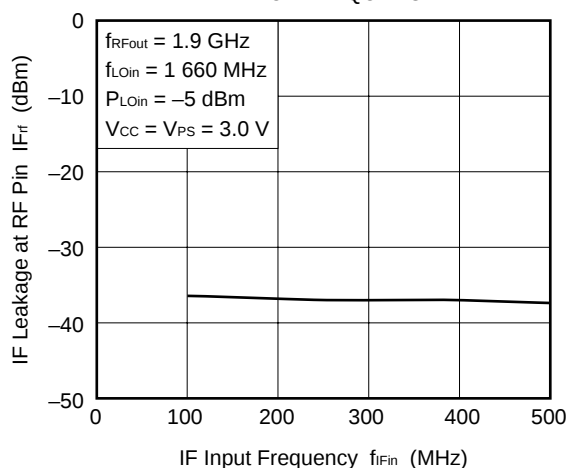
LOCAL LEAKAGE AT RF PIN vs.
LOCAL INPUT FREQUENCY

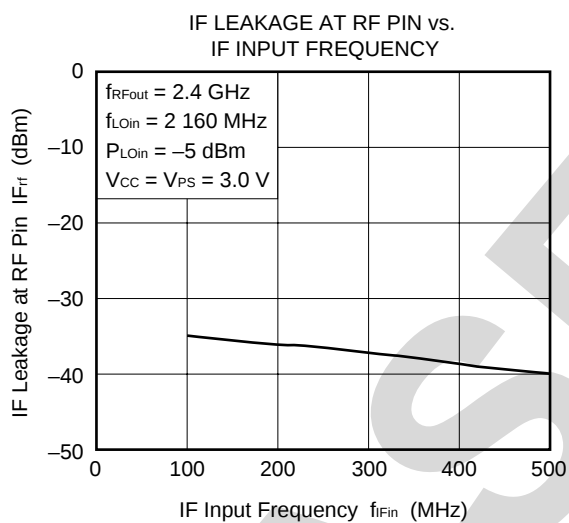
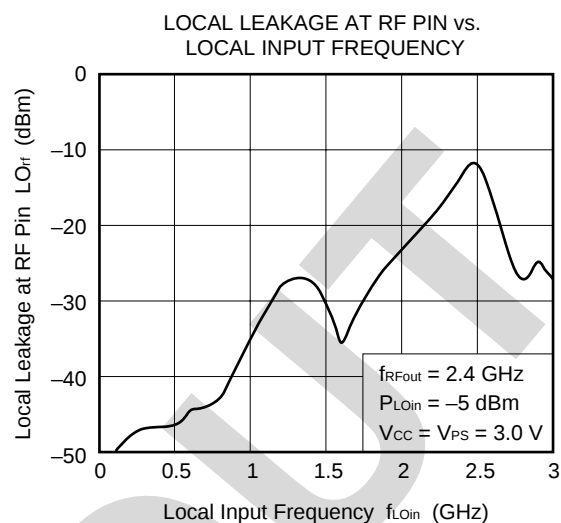
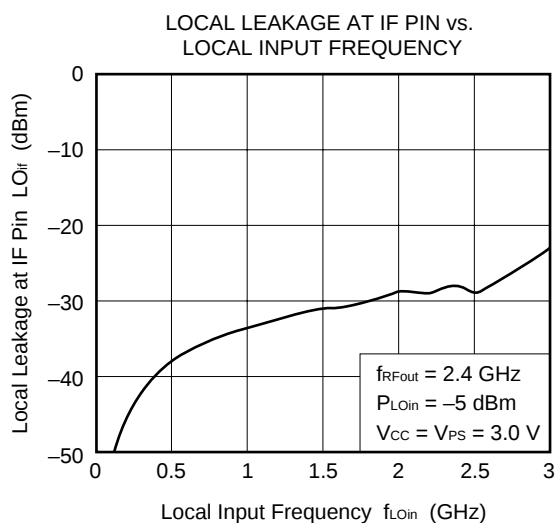


IF LEAKAGE AT RF PIN vs.
IF INPUT FREQUENCY



IF LEAKAGE AT RF PIN vs.
IF INPUT FREQUENCY

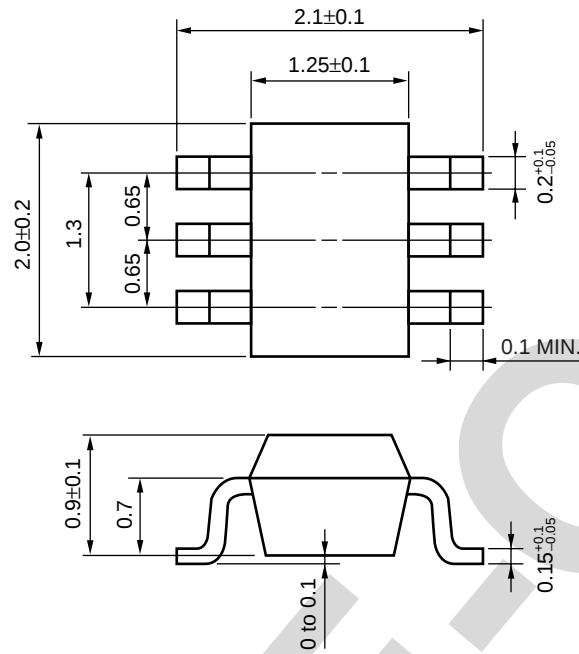




Remark The graphs indicate nominal characteristics.

★ 8. PACKAGE DIMENSIONS

6-PIN SUPER MINIMOLD (UNIT: mm)



9. NOTE ON CORRECT USE

- (1) Observe precautions for handling because of electrostatic sensitive devices.
- (2) Form a ground pattern as wide as possible to minimize ground impedance (to prevent undesired oscillation).
- (3) Connect a bypass capacitor (example: 1 000 pF) to the V_{CC} pin.
- (4) Connect a matching circuit to the RF output pin.
- (5) The DC cut capacitor must be each attached to the input and output pins.

10. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered under the following recommended conditions.

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared Reflow	Package peak temperature: 235°C or below Time: 30 seconds or less (at 210°C) Count: 3, Exposure limit: None ^{Note}	IR35-00-3
VPS	Package peak temperature: 215°C or below Time: 40 seconds or less (at 200°C) Count: 3, Exposure limit: None ^{Note}	VP15-00-3
Wave Soldering	Soldering bath temperature: 260°C or below Time: 10 seconds or less Count: 1, Exposure limit: None ^{Note}	WS60-00-1
Partial Heating	Pin temperature: 300°C Time: 3 seconds or less (per side of device) Exposure limit: None ^{Note}	—

Note After opening the dry pack, keep it in a place below 25°C and 65% RH for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).

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