



THE DATASHEET OF MC14007UBDR2G

Dual Complementary Pair Plus Inverter

Features

- MAXIMUM RATINGS**
- (Voltages Referenced to
- V_{SS}
-)

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V _{DD} +0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P _D	Power Dissipation, per Package (Note 1)	500	mW
T _A	Ambient Temperature Range	−55 to +125	°C
T _{stg}	Storage Temperature Range	−65 to +150	°C
T _L	Lead Temperature (8 second Soldering)	260	°C

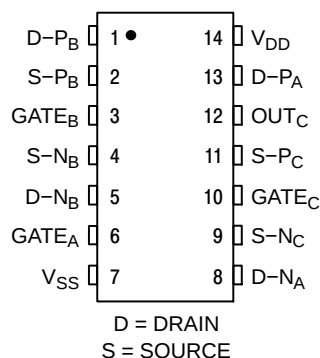
1. Temperature Derating: "D/DW" Package: $-7.0 \text{ mW}/^{\circ}\text{C}$ from 65°C to 125°C .



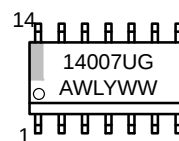
<http://onsemi.com>



PIN ASSIGNMENT



MARKING DIAGRAM



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb-Free Indicator

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

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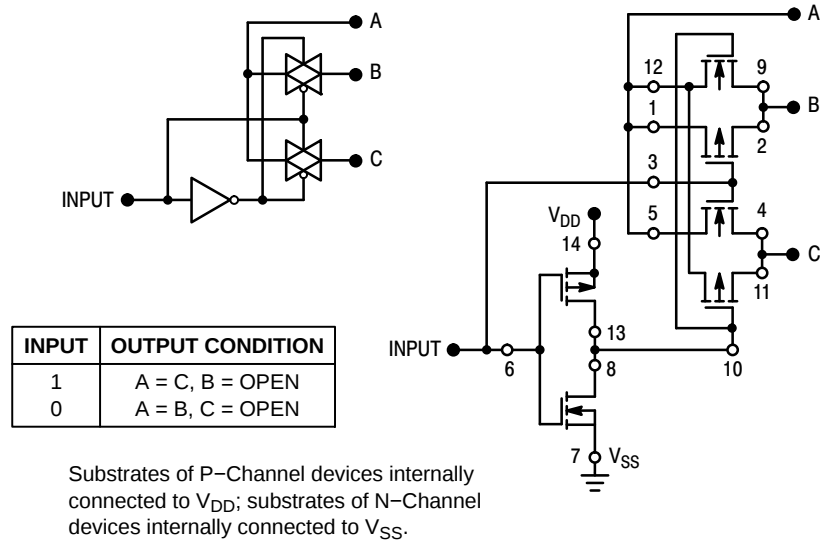


Figure 1. Typical Application: 2-Input Analog Multiplexer

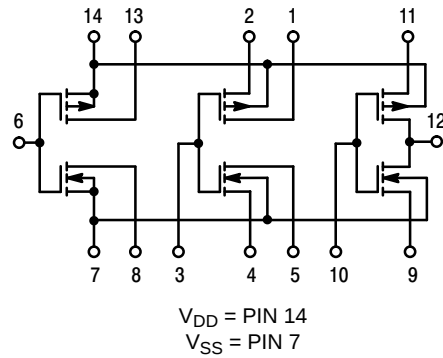


Figure 2. Schematic

MC14007UB

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Symbol	Characteristic	V _{DD} Vdc	–55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (Note 2)	Max	Min	Max	
V _{OL}	Output Voltage V _{in} = V _{DD} or 0	5.0 10 15	– – –	0.05 0.05 0.05	– – –	0 0 0	0.05 0.05 0.05	– – –	0.05 0.05 0.05	Vdc
V _{OH}	V _{in} = 0 or V _{DD}	5.0 10 15	4.95 9.95 14.95	– – –	4.95 9.95 14.95	5.0 10 15	– – –	4.95 9.95 14.95	– – –	Vdc
V _{IL}	Input Voltage (V _O = 4.5 Vdc) (V _O = 9.0 Vdc) (V _O = 13.5 Vdc)	5.0 10 15	– – –	1.0 2.0 2.5	– – –	2.25 4.50 6.75	1.0 2.0 2.5	– – –	1.0 2.0 2.5	Vdc
V _{IH}	(V _O = 0.5 Vdc) (V _O = 1.0 Vdc) (V _O = 1.5 Vdc)	5.0 10 15	4.0 8.0 12.5	– – –	4.0 8.0 12.5	2.75 5.50 8.25	– – –	4.0 8.0 12.5	– – –	Vdc
I _{OH}	Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	5.0 5.0 10 15	–3.0 –0.64 –1.6 –4.2	– – – –	–2.4 –0.51 –1.3 –3.4	–5.0 –1.0 –2.5 –10	– – – –	–1.7 –0.36 –0.9 –2.4	– – – –	mAdc
I _{OL}	(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	5.0 10 15	0.64 1.6 4.2	– – –	0.51 1.3 3.4	1.0 2.5 10	– – –	0.36 0.9 2.4	– – –	mAdc
I _{in}	Input Current	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
C _{in}	Input Capacitance (V _{in} = 0)	–	–	–	–	5.0	7.5	–	–	pF
I _{DD}	Quiescent Current (Per Package)	5.0 10 15	– – –	0.25 0.5 1.0	– – –	0.0005 0.0010 0.0015	0.25 0.5 1.0	– – –	7.5 15 30	μAdc
I _T	Total Supply Current (Notes 3 and 4) (Dynamic plus Quiescent, Per Gate) (C _L = 50 pF)	5.0 10 15	I _T = (0.7 μA/kHz) f + I _{DD} /6 I _T = (1.4 μA/kHz) f + I _{DD} /6 I _T = (2.2 μA/kHz) f + I _{DD} /6							μAdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

4. To calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$

where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and $k = 0.003$.

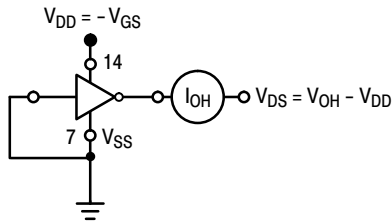
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SWITCHING CHARACTERISTICS (Note 5) ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

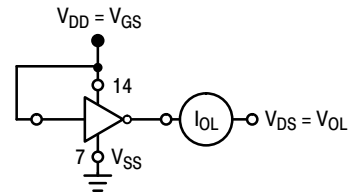
Symbol	Characteristic	V_{DD} Vdc	Min	Typ (Note 6)	Max	Unit
t_{TLH}	Output Rise Time $t_{TLH} = (1.2 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{TLH} = (0.5 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH} = (0.4 \text{ ns/pF}) C_L + 15 \text{ ns}$	5.0 10 15	— — —	90 45 35	180 90 70	ns
t_{THL}	Output Fall Time $t_{THL} = (1.2 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{THL} = (0.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{THL} = (0.4 \text{ ns/pF}) C_L + 10 \text{ ns}$	5.0 10 15	— — —	75 40 30	150 80 60	ns
t_{PLH}	Turn-Off Delay Time $t_{PLH} = (1.5 \text{ ns/pF}) C_L + 35 \text{ ns}$ $t_{PLH} = (0.2 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{PLH} = (0.15 \text{ ns/pF}) C_L + 17.5 \text{ ns}$	5.0 10 15	— — —	60 30 25	125 75 55	ns
t_{PHL}	Turn-On Delay Time $t_{PHL} = (1.0 \text{ ns/pF}) C_L + 10 \text{ ns}$ $t_{PHL} = (0.3 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{PHL} = (0.2 \text{ ns/pF}) C_L + 15 \text{ ns}$	5.0 10 15	— — —	60 30 25	125 75 55	ns

5. The formulas given are for the typical characteristics only. Switching specifications are for device connected as an inverter.

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



All unused inputs connected to ground.



All unused inputs connected to ground.

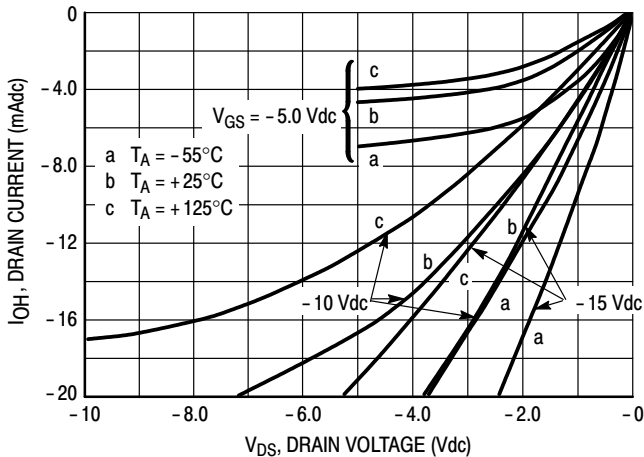


Figure 3. Typical Output Source Characteristics

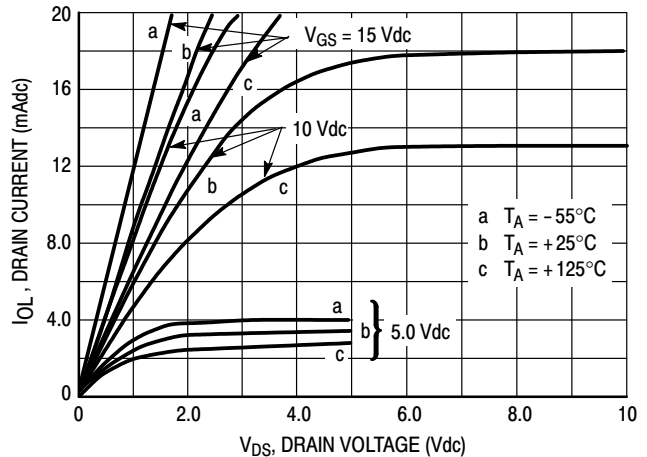


Figure 4. Typical Output Sink Characteristics

These typical curves are not guarantees, but are design aids.
Caution: The maximum current rating is 10 mA per pin.

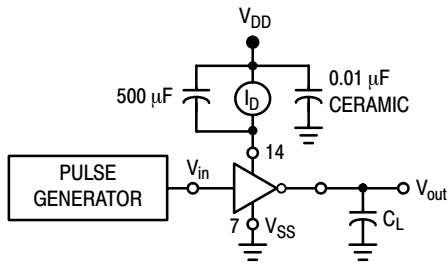
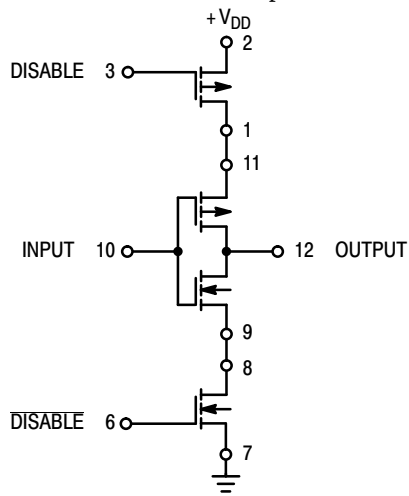


Figure 5. Switching Time and Power Dissipation Test Circuit and Waveforms

APPLICATIONS

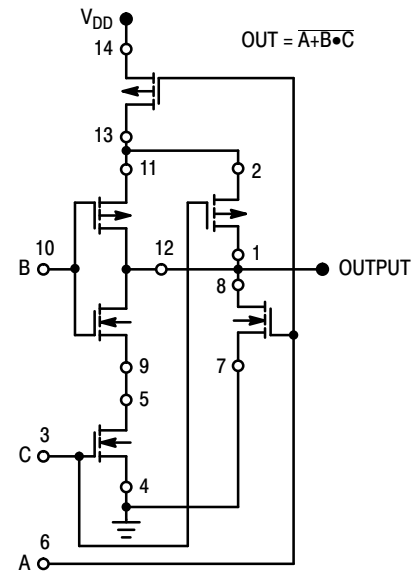
The MC14007UB dual pair plus inverter, which has access to all its elements offers a number of unique circuit applications. Figures 1, 6, and 7 are a few examples of the device flexibility.



INPUT	DISABLE	OUTPUT
1	0	0
0	0	1
X	1	OPEN

X = Don't Care

Figure 6. 3-State Buffer



Substrates of P-Channel devices internally connected to V_{DD} ;
Substrates of N-Channel devices internally connected to V_{SS} .

Figure 7. AOI Functions Using Tree Logic

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ORDERING INFORMATION

Device	Package	Shipping [†]
MC14007UBDG	SOIC-14 (Pb-Free)	55 Units / Rail
MC14007UBDR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
NLV14007UBDR2G*	SOIC-14 (Pb-Free)	2500 / Tape & Reel

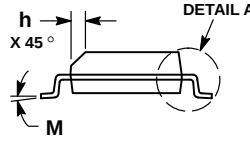
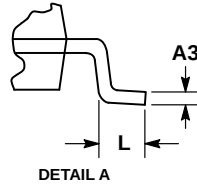
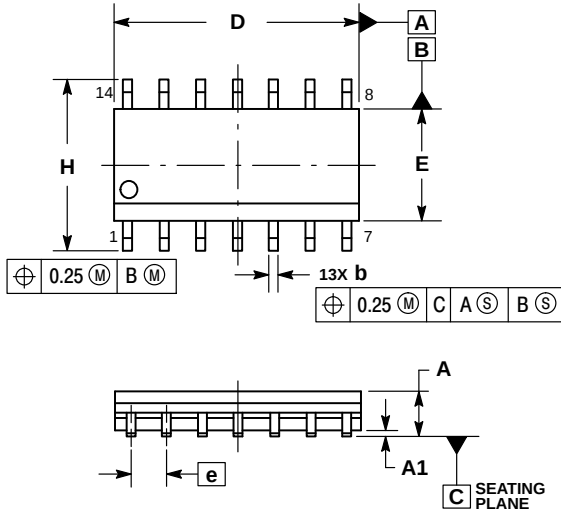
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

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PACKAGE DIMENSIONS

SOIC-14 NB CASE 751A-03 ISSUE K

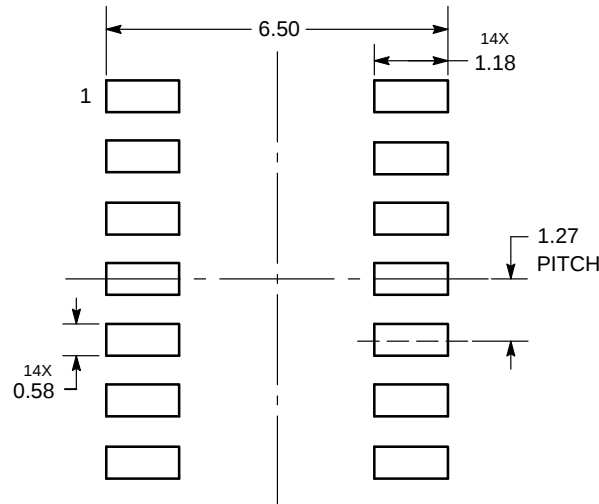


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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