THE DATASHEET OF

FT902Q-T

Future Technology Devices International Ltd.

FT900/1/2/3

(Embedded Microcontroller)

The FT90x series includes the FT900, FT901, FT902 and FT903 which are complete System-On-Chip 32-bit RISC microcontrollers for embedded applications featuring a high level of integration and low power consumption. It has the following features:

- High performance, low power 32-bit FT32 core processor, running at a frequency of 100MHz.
- 256kB on-chip Flash memory.
- 256kB on-chip shadow program memory.
- True Zero Wait States (0WS) up to 3.1 DMIPS per MHz performance
- 64kB on-chip data memory.
- EFUSE for security configuration.
- Integrated Phase-Locked Loop (PLL) supports external 12MHz crystal and direct external clock source input.
- 32.768 kHz real time clock support.
- One USB2.0 EHCI compatible host controller supports high-speed (480 Mbit/s), full-speed (12 Mbit/s), and low-speed (1.5 Mbit/s).
- One USB2.0 peripheral controller supports high-speed (480 Mbit/s) and full-speed (12 Mbit/s).
- USB2.0 host and peripheral controllers support the Isochronous, Interrupt, Control, and Bulk transfers.
- 10/100 Mbps Ethernet that is compliant with the IEEE 802.3/802.3u standards. (FT900 and FT901 only)
- Supports One-Wire debugger for downloading firmware to Flash memory or shadow program memory, and supports a software debugger.
- Two CAN controllers support CAN protocol 2.0 parts A & B, data rate is up to 1 Mbit/s. (FT900 and FT902 only)
- One SPI master supports single / dual / quad modes of data transfer. Clock rate is up to 25 MHz
- Two SPI slaves support single data transfer with 25MHz clock.
- Two I^2C bus interfaces can be configured as master or slave, which support standard / fast / fast plus / high speed mode data transfers. Max data transfer rate up to 3.4 Mbit/s. Clock stretching is supported.
- I^2S bus interface can be configured as master or slave. Two clock input options (24.576 MHz and 22.5792 MHz) to support I^2S master mode for different audio sample rates.
- UART interface can be configured as one full programmable UART0 or two simple interfaces, UART0 and UART1 with CTS / RTS control function.
- Four user timers with pre-scaling and a watchdog function.
- 8-bit parallel data interface supports camera data capturing.
- Support 7 independent PWM channels. Channel 0 and 1 can be configured as PCM 8-bit/16-bit stereo audio output.
- SD host controller is compatible to standard specification V3.0, it supports up to 25 MHz SD clock speed and software supports SD card format in SD/SDHC/SDXC.
- Support two 10-bit DAC 0/1 channels output, sample rate at ~1 MS/s.
- Support seven 10-bit ADC 1/7 channels input, sample rate is up to ~960 kS/s.
- Single 3.3 volt power supply, built-in 1.2 V regulators.
- 3.3 volt I/O power supply.
- Support USB Battery Charging Specification Rev 1.2. Downstream port can be configured as SDP, CDP or DCP. Upstream port can perform BCD mode detection.
- Support VBUS power switching and over current control.
- Power-On Reset (POR).
- -40°C to 85°C extended operating temperature range.
- Available in compact Pb-free 100-Pin packages (all RoHS compliant).

1 Typical Applications

- Home security system
- Home Automation
- Embedded audio application
- Motor drive and application control
- E-meter
- CCTV monitor
- Industrial automation
- Medical appliances
- Instrumentation
- DAQ System

1.1 Part Numbers

Part Number	Package
FT900Q-X	100 Pin QFN, pitch 0.4mm, body 12mm x 12mm x 0.75mm, support both CAN Bus and Ethernet features.
FT900L-X	100 Pin LQFP, pitch 0.5mm, body 14mm x 14mm x 1.40mm, support both CAN Bus and Ethernet features.
FT901Q-X	100 Pin QFN, pitch 0.4mm, body 12mm x 12mm x 0.75mm, support Ethernet, doesn't support CAN Bus.
FT901L-X	100 Pin LQFP, pitch 0.5mm, body 14mm x 14mm x 1.40mm, support Ethernet, doesn't support CAN Bus.
FT902Q-X	100 Pin QFN, pitch 0.4mm, body 12mm x 12mm x 0.75mm, support CAN Bus, doesn't support Ethernet.
FT902L-X	100 Pin LQFP, pitch 0.5mm, body 14mm x 14mm x 1.40mm, support CAN Bus, doesn't support Ethernet.
FT903Q-X	100 Pin QFN, pitch 0.4mm, body 12mm x 12mm x 0.75mm, doesn't support both CAN Bus and Ethernet features.
FT903L-X	100 Pin LQFP, pitch 0.5mm, body 14mm x 14mm x 1.40mm, doesn't support both CAN Bus and Ethernet features.

Table 1-1 FT90x series Part Numbers

Common Interfaces on all packages include: USB Host, USB Peripheral, SPI, UART, ADC, DAC, I2S, PWM, RTC, Timers/Watchdog, Interrupt Controller.

Note: Packaging codes for X is:

-R: Tape and Reel (Qty per reel is 1000)

-T: Tray packing (Qty per tray for LQFP is 90, qty per tray for QFN is 152)

1.2 USB2.0 Compliant

The FT90x series contains a USB2.0 host controller and peripheral controller that both are compliant with USB2.0 specification.

2 FT900 Block Diagram

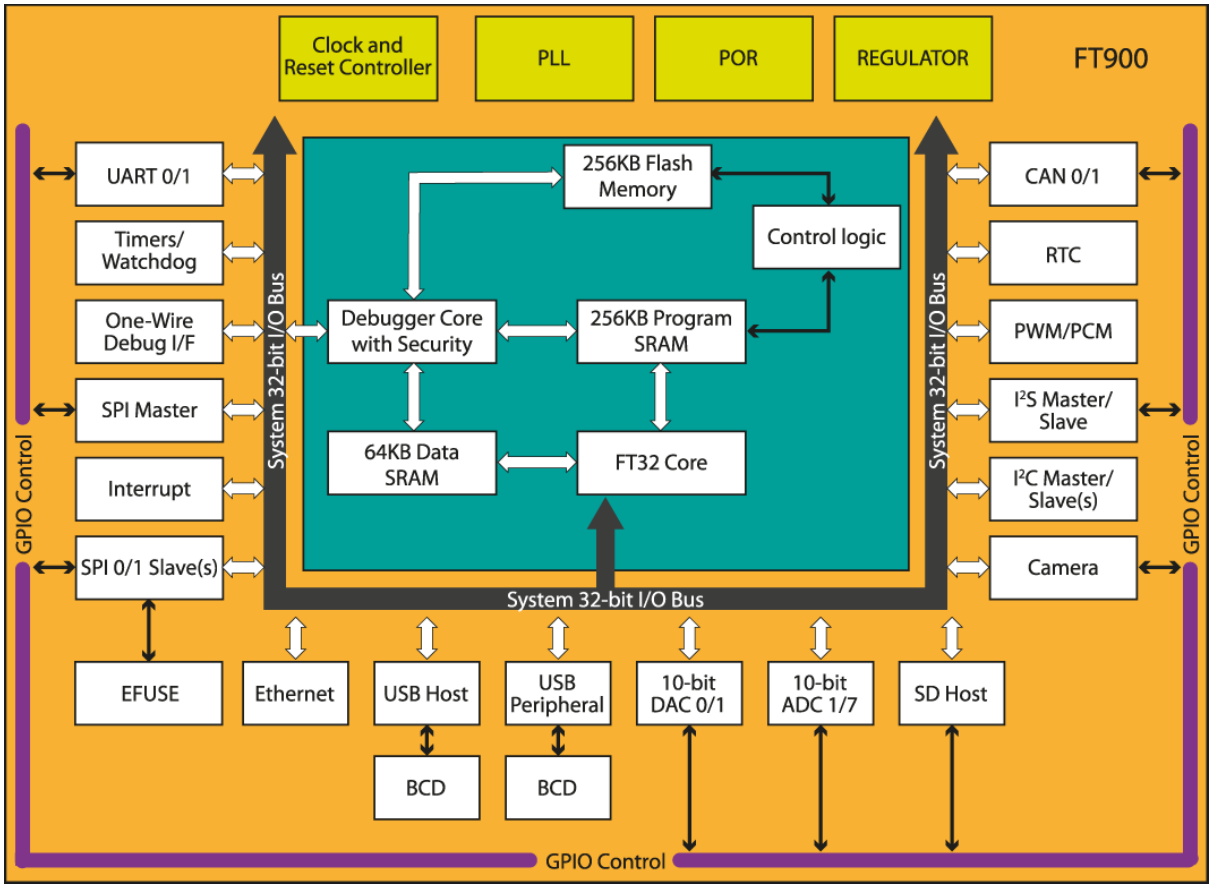


Figure 2-1 FT900 Block Diagram

For a description of each function please refer to Section 5.

Table of Contents

1 Typical Applications 3
1.1 Part Numbers 3
1.2 USB2.0 Compliant 3
2 FT900 Block Diagram 4
3 Device Pin Out and Signal Description 8
3.1 Pin Out – FT900 QFN-100 8
3.2 Pin Out – FT900 LQFP-100 12
3.3 Pin Description 16
4 Function Description 25
4.1 Architectural Overview 25
4.2 FT32 Core Processor 25
4.3 256kB Flash Memory 25
4.4 Boot Sequence 25
4.5 Interrupt 26
4.6 Memory Mapping 27
4.7 USB2.0 Host Controller 28
4.7.1 Features: 28
4.8 USB2.0 Peripheral Contoller 29
4.8.1 Features: 29
4.9 Ethernet Controller 29
4.9.1 Features: 29
4.10 CAN Bus Controller 29
4.10.1 Features: 30
4.11 Real Time Clock 30
4.11.1 Features: 30
4.12 One-Wire Debugger Interface 30
4.12.1 Features: 30
4.13 SPI Interface 30
4.13.1 Features: 30
4.14 I²C Interface 31
4.14.1 Features: 31
4.15 UART Interface 31
4.15.1 Features: 31
4.16 Timers and Watchdog Timer 32
4.16.1 Features: 32
4.17 I²S Interface 32

4.17.1 Features: 32
4.18 Camera Parallel Interface (Data Capture) 32
4.18.1 Features: 33
4.19 PWM 33
4.19.1 Features: 33
4.20 SD host controller 33
4.20.1 Features: 33
4.21 Analog to Digital Converter (ADC) 34
4.21.1 Features: 34
4.22 Digital to Analog Converter (DAC) 34
4.22.1 Features: 34
4.23 General Purpose Input Output 34
4.23.1 Features: 34
4.24 System Clocks 35
4.24.1 12 MHz Oscillator 35
4.24.2 Phase Locked Loop 35
4.24.3 32.768 KHz RTC Oscillator 35
4.24.4 Internal Slow Clock Oscillator 35
4.25 Power Management 35
4.25.1 Power Supply 35
4.25.2 Power Down Mode 36
5 Devices Characteristics and Ratings 37
5.1 Absolute Maximum Ratings 37
5.2 DC Characteristics 38
5.3 AC Characteristics 43
6 Application Information 53
6.1 Crystal Oscillator 53
6.1.1 Crystal oscillator application circuit 53
6.1.2 External clock input 53
6.2 RTC Oscillator 53
6.3 Standard I/O Pin Configuration 54
6.4 USB2.0 Peripheral and Host Interface 55
6.5 10/100 Mb/s Ethernet Interface 56
6.6 Ethernet Connection when Unused (FT900 & FT901) 57
6.7 USB Connection when Unused (FT900_1_2_3) 58
7 Package Parameters 59
7.1 QFN-100 Package Dimensions 59
7.2 QFN-100 Device Marking 60
7.2.1 FT90XQ Top Side 60

7.3 LQFP-100 Package Dimensions 61
7.4 LQFP-100 Device Marking 62
7.4.1 FT90XL Top Side 62
7.5 Solder Reflow Profile 63
8 Abbreviations 64
9 FTDI Chip Contact Information 66
Appendix A – References 67
Appendix B - List of Figures and Tables 67
Appendix C - Revision History 69

3 Device Pin Out and Signal Description

3.1 Pin Out – FT900 QFN-100

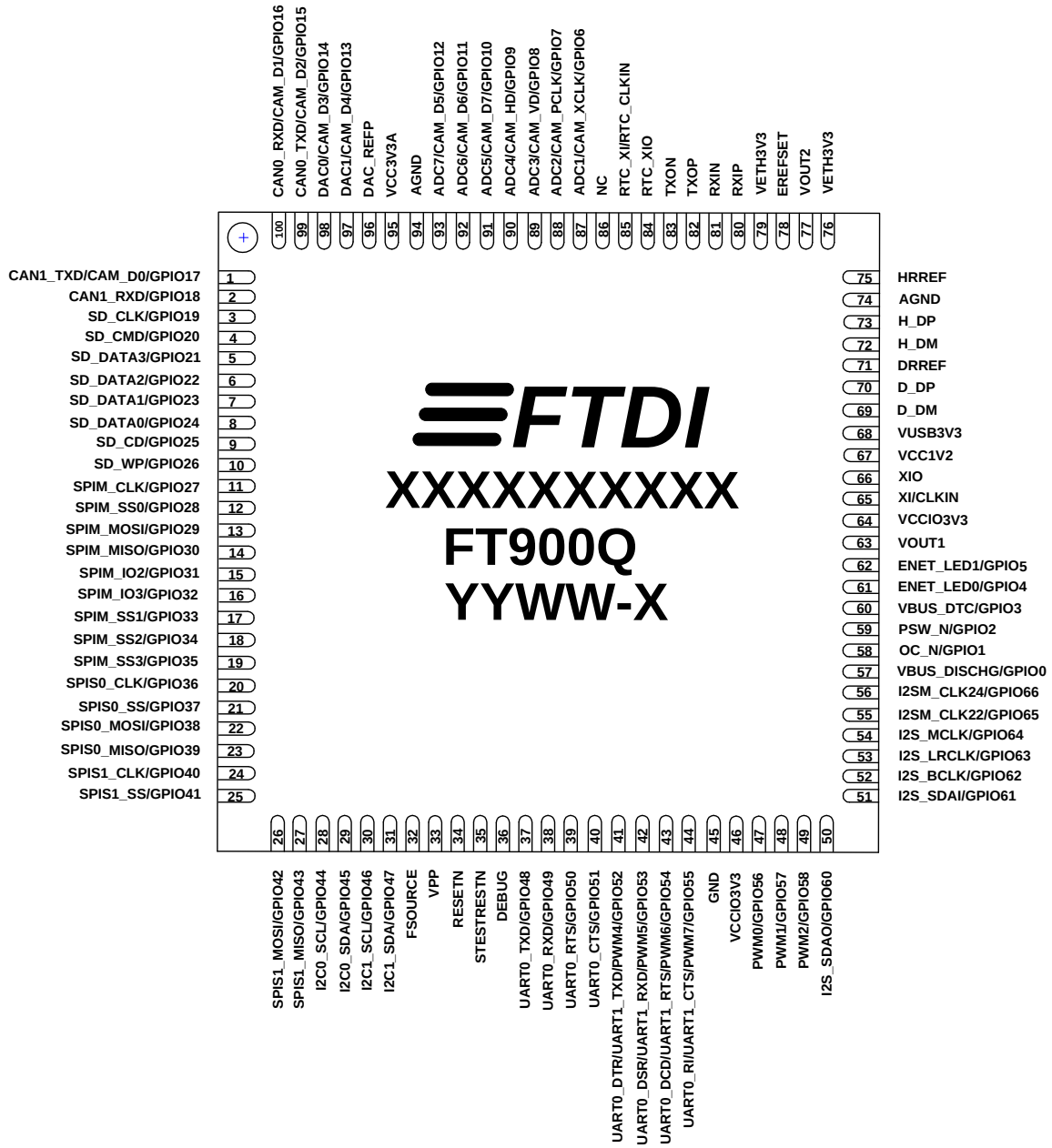


Figure 3-1 Pin Configuration FT900Q (top-down view)

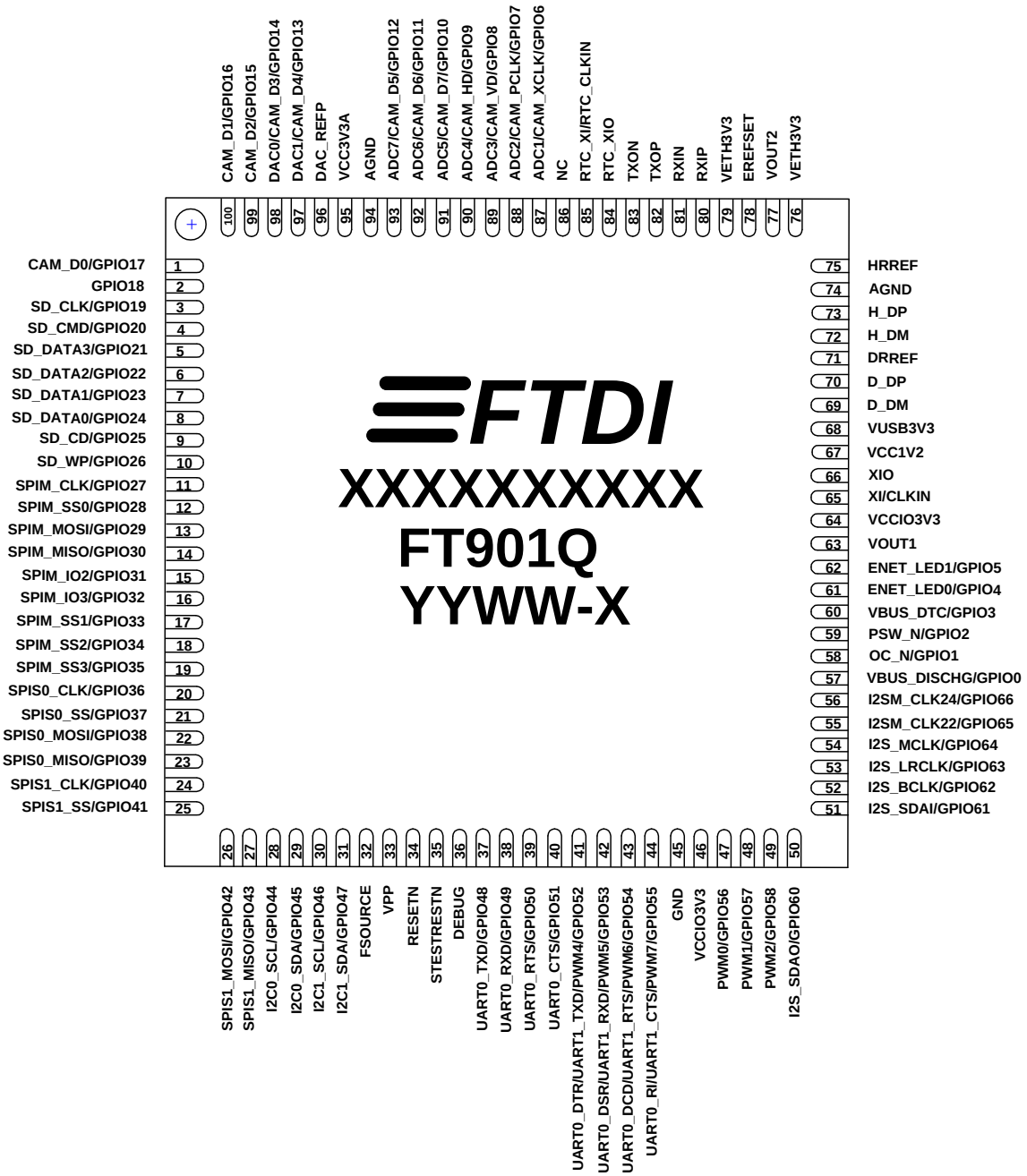


Figure 3-2 Pin Configuration FT901Q (top-down view)

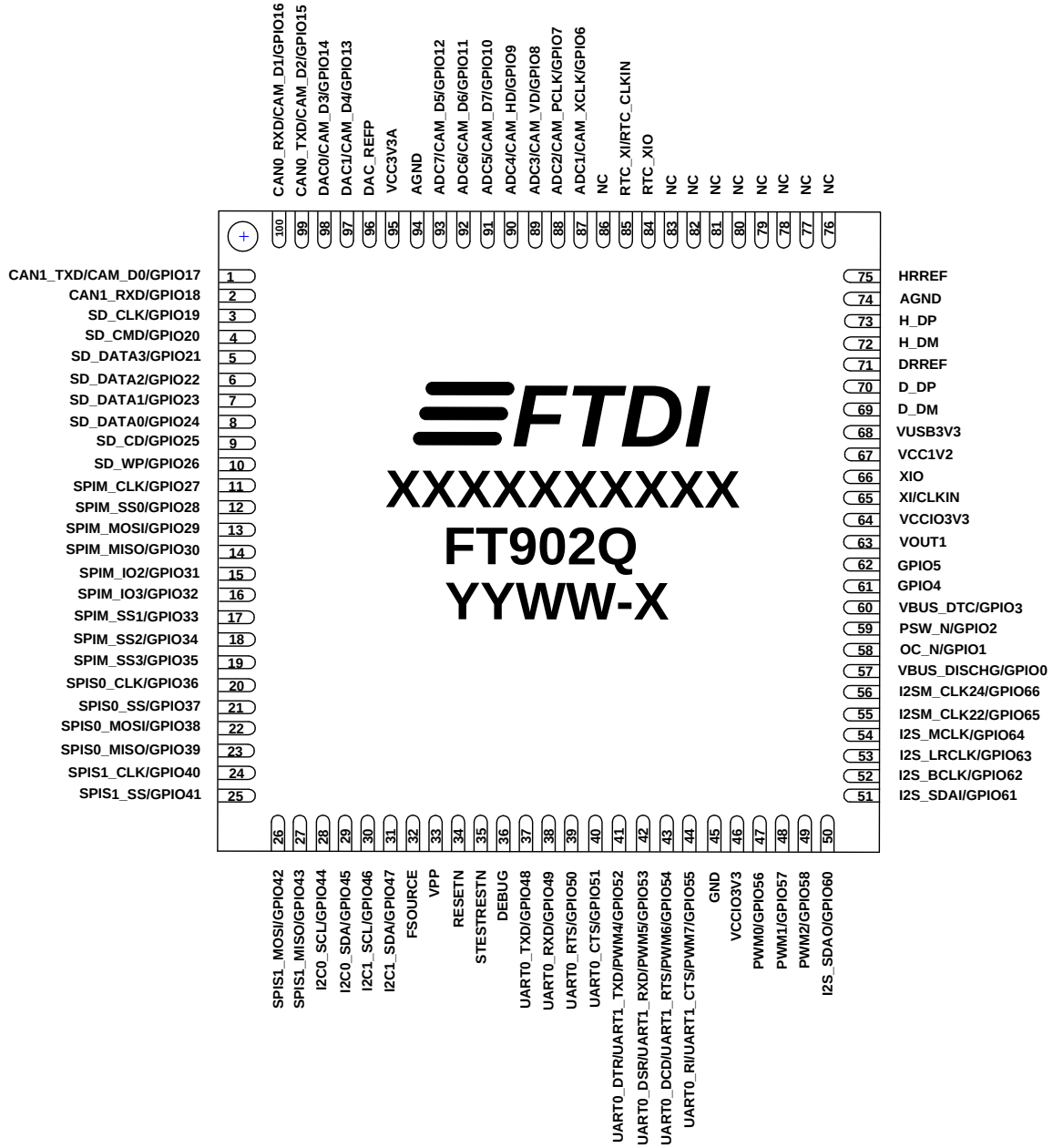


Figure 3-3 Pin Configuration FT902Q (top-down view)

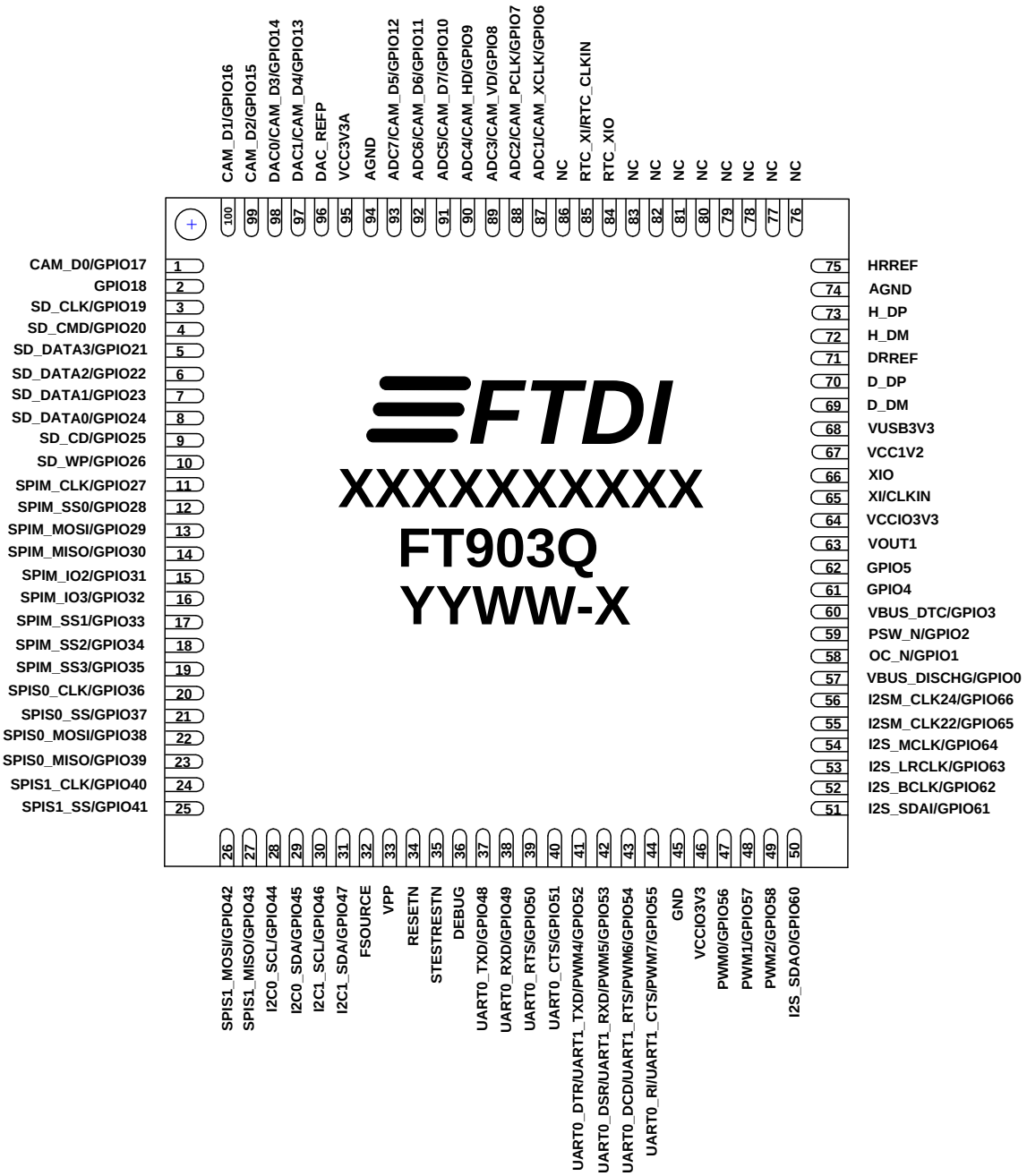


Figure 3-4 Pin Configuration FT903Q (top-down view)

3.2 Pin Out – FT900 LQFP-100

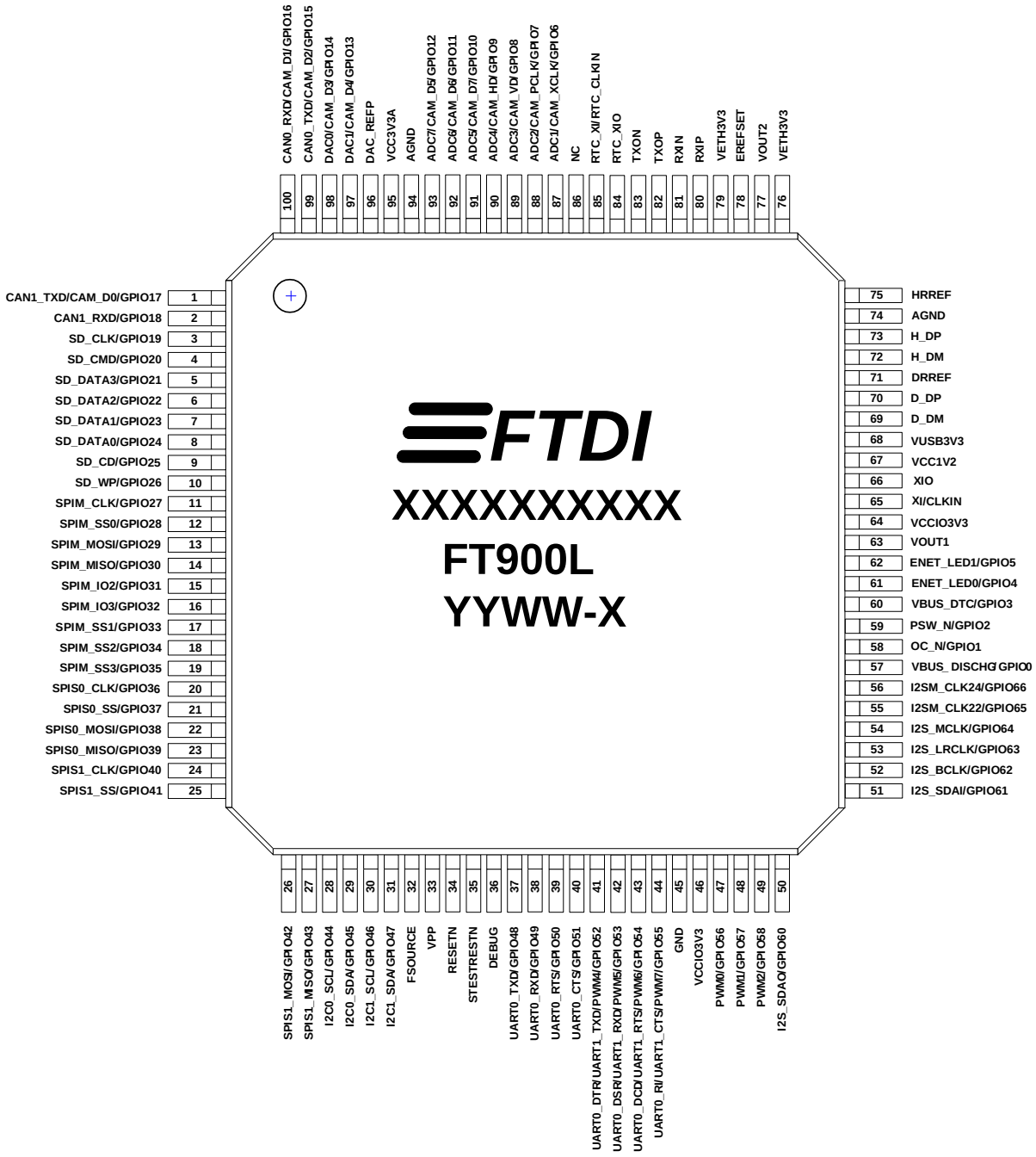


Figure 3-5 Pin Configuration FT900L (top-down view)

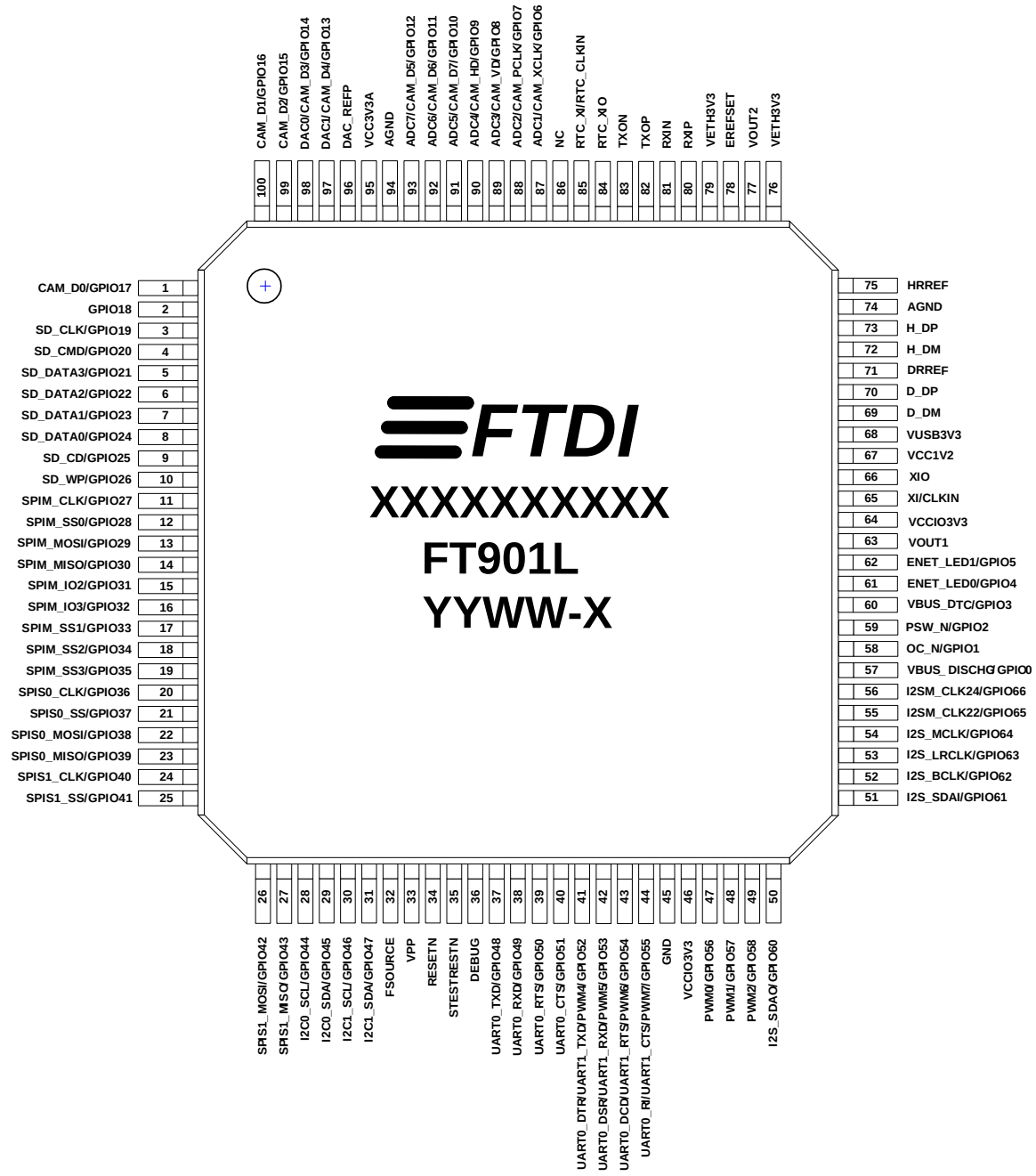


Figure 3-6 Pin Configuration FT901L (top-down view)

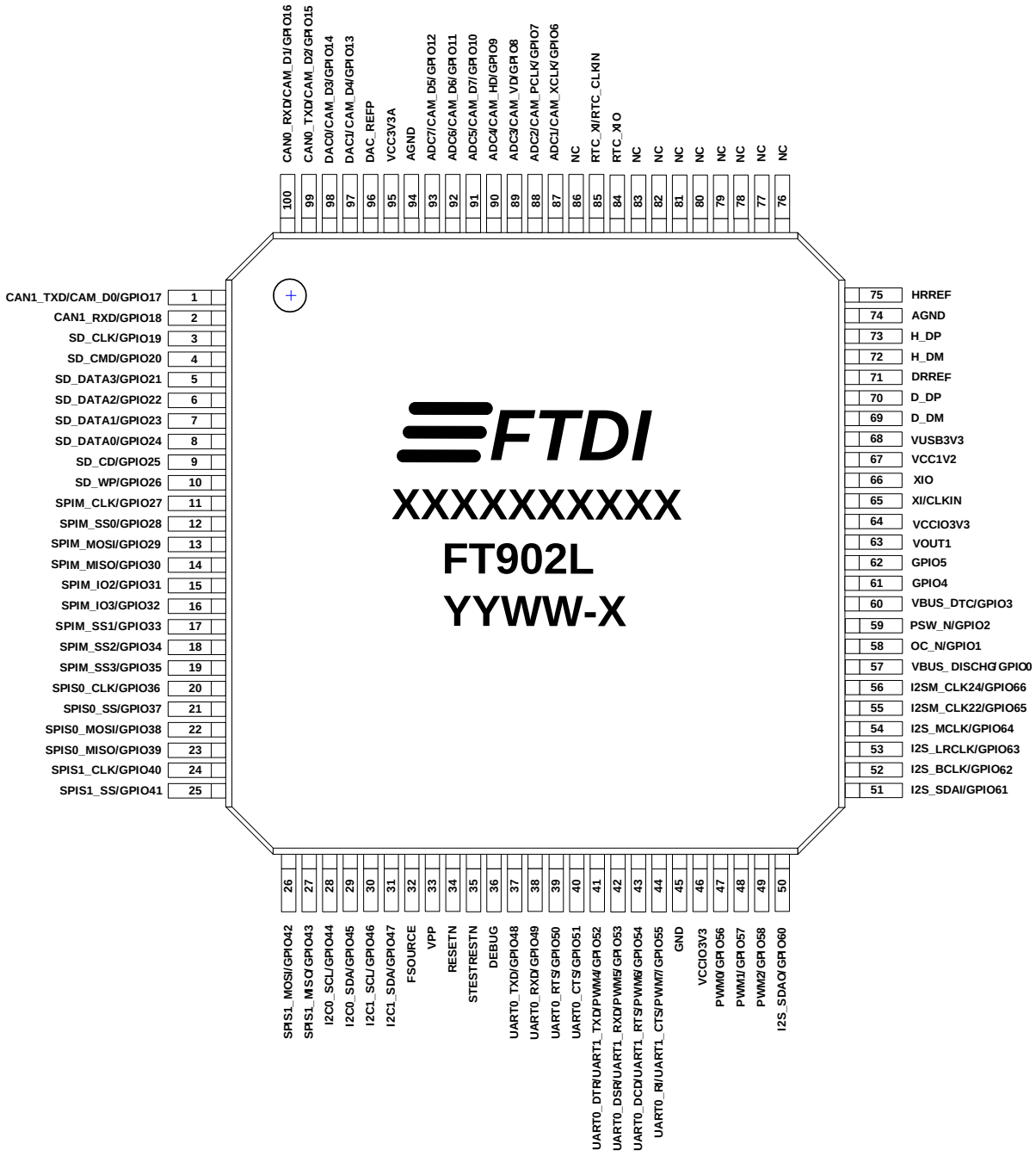


Figure 3-7 Pin Configuration FT902L (top-down view)

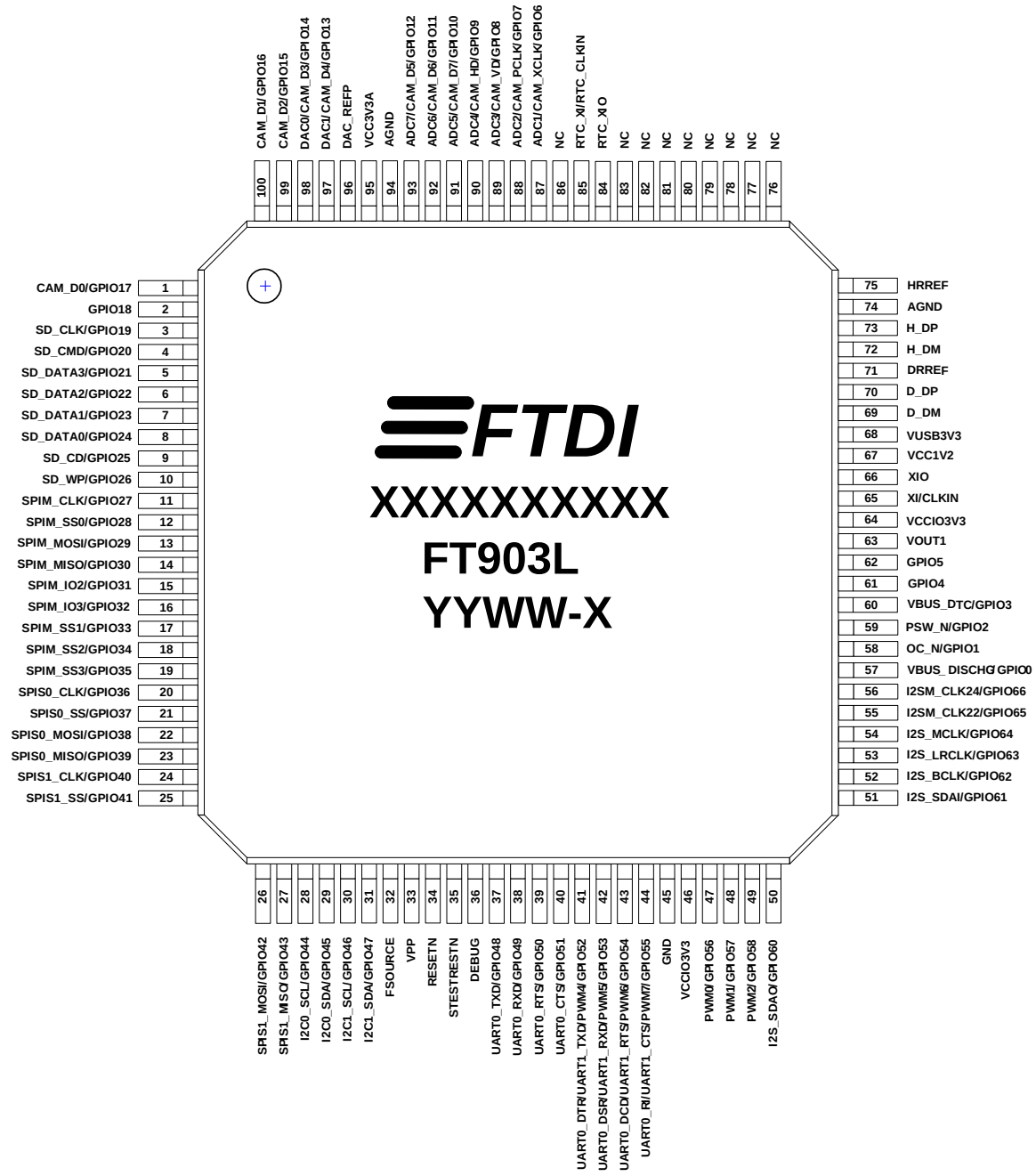


Figure 3-8 Pin Configuration FT903L (top-down view)

3.3 Pin Description

Pin No.	Name	Type	Description
1	CAN1_TXD/CAM_D0/GPIO17	I/O	GPIO17 input/output. (By default is GPIO input, internal pull-low) Camera data 0 input. CAN1 transmitter output. [1]
2	CAN1_RXD/GPIO18	I/O	GPIO18 input/output. (By default is GPIO input, internal pull-low) CAN1 receiver input.[1]
3	SD_CLK/GPIO19	I/O	GPIO19 input/output. (By default is GPIO input, internal pull-low) SD card serial clock output.
4	SD_CMD/GPIO20	I/O	GPIO20 input/output. (By default is GPIO input, internal pull-low) SD card command signal input/output.
5	SD_DATA3/GPIO21	I/O	GPIO21 input/output. (By default is GPIO input, internal pull-low) SD card data bus line 3 input/output.
6	SD_DATA2/GPIO22	I/O	GPIO22 input/output. (By default is GPIO input, internal pull-low) SD card data bus line 2 input/output.
7	SD_DATA1/GPIO23	I/O	GPIO23 input/output. (By default is GPIO input, internal pull-low) SD card data bus line 1 input/output.
8	SD_DATA0/GPIO24	I/O	GPIO24 input/output. (By default is GPIO input, internal pull-low) SD card data bus line 0 input/output.
9	SD_CD/GPIO25	I/O	GPIO25 input/output. (By default is GPIO input, internal pull-low) SD card detect input.
10	SD_WP/GPIO26	I/O	GPIO26 input/output. (By default is GPIO input, internal pull-low) SD card write protection input.
11	SPIM_CLK/GPIO27	I/O	GPIO27 input/output. (By default is GPIO input, internal pull-low) Serial clock output for SPI master.
12	SPIM_SS0/GPIO28	I/O	GPIO28 input/output. (By default is GPIO input, internal pull-low) Slave select 0 output for SPI master.
13	SPIM_MOSI/GPIO29	I/O	GPIO29 input/output. (By default is GPIO input, internal

Pin No.	Name	Type	Description
			pull-low) Master out slave in for SPI master. Data line 0 input/output for SPI master dual & quad mode.
14	SPIM_MISO/GPIO30	I/O	GPIO30 input/output. (By default is GPIO input, internal pull-low) Master in slave out for SPI master. Data line 1 input/output for SPI master dual & quad mode.
15	SPIM_IO2/GPIO31	I/O	GPIO31 input/output. (By default is GPIO input, internal pull-low) Data line 2 input/output for SPI master quad mode.
16	SPIM_IO3/GPIO32	I/O	GPIO32 input/output. (By default is GPIO input, internal pull-low) Data line 3 input/output for SPI master quad mode.
17	SPIM_SS1/GPIO33	I/O	GPIO33 input/output. (By default is GPIO input, internal pull-low) Slave select 1 output for SPI master.
18	SPIM_SS2/GPIO34	I/O	GPIO34 input/output. (By default is GPIO input, internal pull-low) Slave select 2 output for SPI master.
19	SPIM_SS3/GPIO35	I/O	GPIO35 input/output. (By default is GPIO input, internal pull-low) Slave select 3 output for SPI master.
20	SPIS0_CLK/GPIO36	I/O	GPIO36 input/output. (By default is GPIO input, internal pull-low) Serial clock input for SPI slave 0.
21	SPIS0_SS/GPIO37	I/O	GPIO37 input/output. (By default is GPIO input, internal pull-low) Slave select input for SPI slave 0.
22	SPIS0_MOSI/GPIO38	I/O	GPIO38 input/output. (By default is GPIO input, internal pull-low) Master out slave in for SPI slave 0.
23	SPIS0_MISO/GPIO39	I/O	GPIO39 input/output. (By default is GPIO input, internal pull-low) Master in slave out for SPI slave 0.
24	SPIS1_CLK/GPIO40	I/O	GPIO40 input/output. (By default is GPIO input, internal pull-low) Serial clock input for SPI slave 1.
25	SPIS1_SS/GPIO41	I/O	GPIO41 input/output. (By default is GPIO input, internal pull-low)

Pin No.	Name	Type	Description
			Slave select input for SPI slave 1.
26	SPIS1_MOSI/GPIO42	I/O	GPIO42 input/output. (By default is GPIO input, internal pull-low) Master out slave in for SPI slave 1.
27	SPIS1_MISO/GPIO43	I/O	GPIO43 input/output. (By default is GPIO input, internal pull-low) Master in slave out for SPI slave 1.
28	I2C0_SCL/GPIO44	I/O	GPIO44 input/output. (By default is GPIO input, internal pull-low) I^2C 0 serial clock input/output. (By default is I^2C 0 master)
29	I2C0_SDA/GPIO45	I/O	GPIO45 input/output. (By default is GPIO input, internal pull-low) I^2C 0 data line input/output. (By default is I^2C 0 master)
30	I2C1_SCL/GPIO46	I/O	GPIO46 input/output. (By default is GPIO input, internal pull-low) I^2C 1 serial clock input/output. (By default is I^2C 1 slave)
31	I2C1_SDA/GPIO47	I/O	GPIO47 input/output. (By default is GPIO input, internal pull-low) I^2C 1 data line input/output. (By default is I^2C 1 slave)
32	FSOURCE	I	EFUSE Program source input (3.6V-3.8V). If not used for EFUSE programming, leave this pin floating or short to Ground.
33	VPP	I	EFUSE Program source input (1.8V-1.9V). If not used for EFUSE programming, leave this pin floating.
34	RESETN	I	Chip reset input for normal operation. Active low. Connect external 10k pull-up to VCC3V3 for safe operation.
35	STESTRESETN	I	Chip reset input for test mode. Short to Ground for normal operation.
36	DEBUG	I/O	One-wire debugger interface input/output.
37	UART0_TXD/GPIO48	I/O	GPIO48 input/output. (By default is GPIO input, internal pull-low) Transmitter output for UART0.
38	UART0_RXD/GPIO49	I/O	GPIO49 input/output. (By default is GPIO input, internal pull-low) Receiver input for UART0.
39	UART0_RTS/GPIO50	I/O	GPIO50 input/output. (By default is GPIO input, internal pull-low)

Pin No.	Name	Type	Description
			Request to send output for UART0.
40	UART0_CTS/GPIO51	I/O	GPIO51 input/output. (By default is GPIO input, internal pull-low) Clear to send input for UART0.
41	UART0_DTR/UART1_TXD/ PWM4/GPIO52	I/O	GPIO52 input/output. (By default is GPIO input, internal pull-low) PWM channel 4, output. Transmitter output for UART1. Data terminal ready output for UART0.
42	UART0_DSR/UART1_RXD/ PWM5/GPIO53	I/O	GPIO53 input/output. (By default is GPIO input, internal pull-low) PWM channel 5, output. Receiver input for UART1. Data set ready input for UART0.
43	UART0_DCD/UART1_RTS/ PWM6/GPIO54	I/O	GPIO54 input/output. (By default is GPIO input, internal pull-low) PWM channel 6, output. Request to send output for UART1. Data carrier detection input for UART0.
44	UART0_RI/UART1_CTS/ PWM7/GPIO55	I/O	GPIO55 input/output. (By default is GPIO input, internal pull-low) PWM channel 7, output. Clear to send input for UART1. Ring indicator input for UART0.
45	GND	P	Ground
46	VCCIO3V3	P	+3.3V supply voltage. This is the supply voltage for all the I/O ports. Connect 10uF and 0.1uF decoupling capacitors to GND. This pin must be connected to pin 64.
47	PWM0/GPIO56	I/O	GPIO56 input/output. (By default is GPIO input, internal pull-low) PWM channel 0, output. A stereo 16/8-bit PCM audio data channel output.
48	PWM1/GPIO57	I/O	GPIO57 input/output. (By default is GPIO input, internal pull-low) PWM channel 1, output. A stereo 16/8-bit PCM audio data channel output.
49	PWM2/GPIO58	I/O	GPIO58 input/output. (By default is GPIO input, internal pull-low)

Pin No.	Name	Type	Description
			PWM channel 2, output.
50	I2S_SDAO/GPIO60	I/O	GPIO60 input/output. (By default is GPIO input, internal pull-low) Serial data line output for I2S master or slave.
51	I2S_SDAI/GPIO61	I/O	GPIO61 input/output. (By default is GPIO input, internal pull-low) Serial data line input for I2S master or slave.
52	I2S_BCLK/GPIO62	I/O	GPIO62 input/output. (By default is GPIO input, internal pull-low) Bit clock line output for I2S master transmitter or input for I2S slave receiver.
53	I2S_LRCLK/GPIO63	I/O	GPIO63 input/output. (By default is GPIO input, internal pull-low) Left / Right clock line output for I2S master transmitter or input for I2S slave receiver.
54	I2S_MCLK/GPIO64	I/O	GPIO64 input/output. (By default is GPIO input, internal pull-low) I2S master transmitter clock output.
55	I2SM_CLK22/GPIO65	I/O	GPIO65 input/output. (By default is GPIO input, internal pull-low) I2S master external 22.5792MHz clock input.
56	I2SM_CLK24/GPIO66	I/O	GPIO66 input/output. (By default is GPIO input, internal pull-low) I2S master external 24.576MHz clock input.
57	VBUS_DISCHG/GPIO0	I/O	GPIO0 input/output. (By default is GPIO input, internal pull-high) USB host VBUS discharge.
58	OC_N/GPIO1	I/O	GPIO1 input/output. (By default is GPIO input, internal pull-high) USB host port over current status output. Active low.
59	PSW_N/GPIO2	I/O	GPIO2 input/output. (By default is GPIO input, internal pull-high) USB host port external VBUS power switcher. Active low.
60	VBUS_DTC/GPIO3	I/O	GPIO3 input/output. (By default is GPIO input, internal pull-low) USB peripheral VBUS detection.
61	ENET_LED0/GPIO4	I/O	GPIO4 input/output. (By default is GPIO input, internal pull-low) Ethernet activity indicator LED 0.[2]

Pin No.	Name	Type	Description
62	ENET_LED1/GPIO5	I/O	GPIO5 input/output. (By default is GPIO input, internal pull-low) Ethernet activity indicator LED 1.[2]
63	VOUT1	P	+1.2V Regulator power output. This is internal regulator output. Connect 4.7uF and 0.1uF decoupling capacitors to GND. This pin must be connected to pin 67.
64	VCCIO3V3	P	+3.3V supply voltage. This is the supply voltage for all the I/O ports. Connect a 0.1uF decoupling capacitor. This pin must be connected to pin 46.
65	XI/CLKIN	AI	12MHz clock frequency input to the Oscillator circuit or to internal clock generator circuit.
66	XIO	AO	Output from the Oscillator amplifier.
67	VCC1V2	P	+1.2V Regulator power supply for USB. Provide +1.2V power to this pin. This pin must be connected to pin 63. Connect 0.1uF decoupling capacitor.
68	VUSB3V3	P	+3.3V supply voltage. This is the supply voltage for USB peripheral and host I/O ports. Connect 10uF and 0.1uF decoupling capacitors. This pin could be connected to all +3.3V power supply pins without 10uF capacitor.
69	D_DM	AI/O	USB peripheral bidirectional DM line.
70	D_DP	AI/O	USB peripheral bidirectional DP line.
71	DRREF	AI	USB peripheral reference voltage input. Connect 12Kohm +/- 1% resistor to GND.
72	H_DM	AI/O	USB host bidirectional DM line.
73	H_DP	AI/O	USB host bidirectional DP line.
74	AGND	P	Analog Ground
75	HRREF	AI	USB host reference voltage input. Connect 12Kohm +/- 1% resistor to GND.
76	VETH3V3	P	+3.3V supply voltage. This is the supply voltage for Ethernet I/O ports. Connect 10uF and 0.1uF decoupling capacitors. This pin could be connected to all +3.3V power supply pins without 10uF capacitor.
77	VOUT2	P	+1.2V Regulator power supply.[2] This is an internal regulator output. Connect 0.1uF

Pin No.	Name	Type	Description
			decoupling capacitors.
78	EREFSET	AI	Ethernet reference voltage input.[2] Connect 12.3Kohm +/- 1% resistor to GND.
79	VETH3V3	P	+3.3V supply voltage. This is the supply voltage for Ethernet I/O ports. Connect a 0.1uF decoupling capacitor. This pin must be connected to pin 76.
80	RXIP	I	Ethernet receive data positive input.[2] Differential receive signal pair.
81	RXIN	I	Ethernet receive data negative input.[2] Differential receive signal pair.
82	TXOP	O	Ethernet transmit data positive output.[2] Differential transmit signal pair.
83	TXON	O	Ethernet transmit data negative output.[2] Differential transmit signal pair.
84	RTC_XIO	AO	Output from the RTC Oscillator amplifier.
85	RTC_XI/RTC_CLKIN	AI	32.768KHz clock frequency input to the RTC Oscillator circuit or to internal RTC clock generator circuit.
86	NC	-	Not connected.
87	ADC1/CAM_XCLK/GPIO6	I/O	GPIO6 input/output. (By default is GPIO input, internal pull-low) Camera external clock output. 10-bit A/D converter 1, input.
88	ADC2/CAM_PCLK/GPIO7	I/O	GPIO7 input/output. (By default is GPIO input, internal pull-low) Camera pixel clock input. 10-bit A/D converter 2, input.
89	ADC3/CAM_VD/GPIO8	I/O	GPIO8 input/output. (By default is GPIO input, internal pull-low) Camera vertical sync input. 10-bit A/D converter 3, input.
90	ADC4/CAM_HD/GPIO9	I/O	GPIO9 input/output. (By default is GPIO input, internal pull-low) Camera horizontal reference input. 10-bit A/D converter 4, input.
91	ADC5/CAM_D7/GPIO10	I/O	GPIO10 input/output. (By default is GPIO input, internal pull-low)

Pin No.	Name	Type	Description
			Camera data 7 input. 10-bit A/D converter 5, input.
92	ADC6/CAM_D6/GPIO11	I/O	GPIO11 input/output. (By default is GPIO input, internal pull-low) Camera data 6 input. 10-bit A/D converter 6, input.
93	ADC7/CAM_D5/GPIO12	I/O	GPIO12 input/output. (By default is GPIO input, internal pull-low) Camera data 5 input. 10-bit A/D converter 7, input.
94	AGND	P	Analog Ground
95	VCC3V3A	P	+3.3V supply voltage. This is the supply voltage for Analog I/O ports. Connect 10uF and 0.1uF decoupling capacitors. This pin could be connected to all VCC3V3 pins without 10uF capacitor.
96	DAC_REFP	I	10-bit DAC positive reference voltage.
97	DAC1/CAM_D4/GPIO13	I/O	GPIO13 input/output. (By default is GPIO input, internal pull-low) Camera data 4 input. 10-bit D/A converter 1, output.
98	DAC0/CAM_D3/GPIO14	I/O	GPIO14 input/output. (By default is GPIO input, internal pull-low) Camera data 3 input. 10-bit D/A converter 0, output.
99	CAN0_TXD/CAM_D2/GPIO15	I/O	GPIO15 input/output. (By default is GPIO input, internal pull-low) CAN0 transmitter output. [1] Camera data 2 input.
100	CAN0_RXD/CAM_D1/GPIO16	I/O	GPIO16 input/output. (By default is GPIO input, internal pull-low) CAN0 receiver input. [1] Camera data 1 input.

Table 3-1 FT900 pin description

[1] CAN Bus 0/1 only are featured on both FT900 and FT902 packages.

[2] Ethernet pins are available on FT900 and FT901 only. For FT902 and FT903, shall leave all Ethernet pins as NC pin floating except for pin61 and pin62 as GPIO by default.

Notes:

P : Power or ground I : Input

O	: Output	AI	: Analog Input
OD	: Open drain output	AO	: Analog Output
I/O	: Bi-direction Input and Output	AI/O	: Analog Input / Output

4 Function Description

4.1 Architectural Overview

The FT90x series embedded microcontrollers include a high performance 32-bit FT32 RISC core processor and 256kB hi-speed Flash memory for software program downloading with a One-Wire debugger interface. The core processor uses a 32-bit I/O system bus to connect to all of the peripherals.

- USB2.0 host controller
- USB2.0 peripheral controller
- 10/100Mbps Ethernet controller *(FT900 and FT901 only)*
- Two CAN bus interfaces *(FT900 and FT902 only)*
- Real Time Clock
- One-Wire debugger interface
- One SPI master interface and two SPI slave interfaces
- Two I^2C bus interfaces
- One I^2S bus interface
- UART interface
- Four timers and a 32-bit watchdog timer
- Camera parallel interface
- SD host controller
- PWM motor controller
- 10-bit DAC0/1 channel
- 10-bit ADC1-7 channel
- General purpose I/O interface

The functions for each controller / interface are briefly described in the following subsections.

4.2 FT32 Core Processor

The FT32 core processor is running at frequencies of up to 100MHz. The processor contains the CPU itself with control logic and its 256kB program memory and 64kB data memory. The outside connections for the core processor are the memory-mapped I/O interface, the interrupt interface, asynchronous reset and the system clock.

4.3 256kB Flash Memory

The internal 256kB Flash memory is used to store a boot loader or user application of the FT90x series. It is a high performance and low power consumption memory that supports upto 80MHz serial clock. The system will perform memory copy from Flash memory to CPU program memory automatically after system power on.

4.4 Boot Sequence

After the initial memory copy completes, the CPU jumps to program memory location zero. This may be the start of the user application which is stored in advance in Flash memory, or a boot loader only which allows program memory to perform modification via (e.g.) UART or USB.

The option of a boot loader is a special purpose routine in the FT90x series embedded microcontroller. It is a small routine stored in the Flash memory. Typically the boot loader is 1-4kbytes in size, and is loaded at the top of the available memory.

4.5 Interrupt

The FT900 interrupt controller handles 32 interrupt inputs. When an interrupt occurred, the Interrupt Service Route (ISR) will process this event via the CPU. The ISR vector range is from 0 to 31, which corresponds to interrupt 0 to 31. See Table 4-1 information.

Each interrupt shall be assigned the interrupt vector number and priority before use. By default, the highest priority interrupt is interrupt 0, and the lowest is interrupt 31. However, the interrupt priority can be rearranged by register settings and also allows multiple interrupts at the same priority.

To prevent the loss and delay of high priority interrupts, the FT90x series uses nested interrupts if enabled. Nested interrupts allow interrupt requests of a high priority to pre-empt interrupt requests of a lower priority. FT90x series supports up to 16-levels deep of nested interrupts.

The interrupt controller has a global interrupt mask bit to temporarily block all interrupts. If this bit is set to "1", then with the exception of an interrupt assigned priority as "0", which is a non-maskable interrupt (NMI) input, all interrupts are masked.

See Table 4-2 for FT90x series default interrupt priority.

Peripherals of Interrupt	Interrupt Vector Index	Default Priority
Power Management	0	0 (NMI)
USB2.0 Host Controller	1	1
USB2.0 Peripheral Controller	2	2
Ethernet Controller	3	3
SD Host Controller	4	4
CAN Bus 0	5	5
CAN Bus 1	6	6
Camera	7	7
SPI Master	8	8
SPI Slave 0	9	9
SPI Slave 1	10	10
I^2C 0	11	11
I^2C 1	12	12
UART 0	13	13
UART 1	14	14
I^2S Bus	15	15
PWM	16	16
Timers	17	17
GPIO	18	18

Peripherals of Interrupt	Interrupt Vector Index	Default Priority
RTC	19	19
ADC	20	20
DAC	21	21
Slow Clock Timer	22	22
UNUSED	**23-31**	**23-31**

Table 4-1 FT90x series default interrupt priority

4.6 Memory Mapping

A list of the I/O memory mapping for registers and memory in the FT90x series is given below in table 4-2. Please refer to FT900 User Manual for detail description of registers.

Function	Address Memory Range		Comment
General setup registers	0x10000	0x100BF	DW/W/B
Interrupt controller registers	0x100C0	0x100FF	DW/W/B
USB2.0 host controller registers	0x10100	0x1017F	DW/W/B
USB2.0 host controller RAM memory	0x11000	0x12FFF	DW/W/B
USB2.0 peripheral controller registers	0x10180	0x1021F	DW/W/B
Ethernet controller registers	0x10220	0x1023F	DW/W/B (Uses DW to access FIFO)
CAN BUS 0 registers	0x10240	0x1025F	B
CAN BUS 1 registers	0x10260	0x1027F	B
RTC registers	0x10280	0x1029F	DW
SPI master registers	0x102A0	0x102BF	DW
SPI slave 0 registers	0x102C0	0x102DF	DW
SPI slave 1 registers	0x102E0	0x102FF	DW
I^2C master registers	0x10300	0x1030F	B (I2C 0 and I2C 1 both can be configure as master or slave)
I^2C slave registers	0x10310	0x1031F	B (I2C 0 and I2C 1 both can be configure as master or slave)
UART 0 register	0x10320	0x1032F	B

Function	Address Memory Range		Comment
UART 1 registers	0x10330	0x1033F	B
Timers (include Watchdog) registers	0x10340	0x1034F	B
I^2S master or slave registers	0x10350	0x1035F	W
Camera registers	0x10360	0x1036F	DW
Reserved	0x10370	0x103BF	-
PWM registers	0x103C0	0x103FF	Registers: B access FIFO: W access
SD host controller registers	0x10400	0x107FF	DW
Flash controller registers	0x10800	0x108BF	B
Reserved	0x108C0	0x10FFF	-

Table 4-2 FT90x series I/O memory mapping

Notes: DW / W / B are length of register operation.

DW: Double Word (32-bit) W: Word (16-bit) B: Byte (8-bit)

4.7 USB2.0 Host Controller

The Hi-Speed USB2.0 single-port host controller is compliant with the USB2.0 specification and the Enhanced Host Controller Interface (EHCI) specification. There is an option to enable a downstream port with a Battery Charging (BC) feature, which can be configured as Standard Downstream Port (SDP), or Charging Downstream Port (CDP), or Dedicated Charging Port (DCP). The battery charging feature is compatible with the Battery Charging Specification Revision 1.2 (BC 1.2) by USB-IF.

4.7.1 Features:

- Compliant with the USB specification revision 2.0.
- Compliant with EHCI specification revision 1.0.
- The USB1.1 host is integrated into the USB2.0 EHCI compatible host controller.
- Supports data transfer at hi-speed (480 Mbit/s), full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s).
- Supports the split transaction for hi-speed Hubs and the preamble transaction full-speed hubs.
- Supports the Isochronous/Interrupt/Control/Bulk data transfers.
- 8kB high speed RAM memory integrated.
- Supports Battery Charging specification revision 1.2.
- Supports VBUS power switching and over current control.

4.8 USB2.0 Peripheral Contoller

The USB 2.0 peripheral controller is fully compliant with the USB2.0 specification. There is also an option to enable a battery charger detection (BCD) feature on the upstream port, which can identify whether the connected downstream port supports SDP, CDP or DCP charging function. Battery charge detection allows the USB device to determine if higher currents may be available from the USB connection for rapid battery charging.

4.8.1 Features:

- Supports data transfer at hi-speed (480 Mbit/s) and full-speed (12 Mbit/s).
- Software configurable EP0 control endpoint size 8-64 bytes
- Software configurable 7 IN/OUT endpoints.
- EP1-EP7 has double buffering which contains 2kB IN and 2kB OUT buffers.
- Supports the Isochronous/Interrupt/Control/Bulk data transfers.
- Max endpoint packet sizes upon 1024 bytes.
- Supports VBUS detection.
- Supports suspend and resume power management functions.
- Supports remote wakeup feature.
- Supports Battery Charging specification revision 1.2.

4.9 Ethernet Controller

The Ethernet controller contains an on-chip 10/100BASE-TX Ethernet transceiver and Media Access Control (MAC) designed to provide high performance of frame transmission and reception. The Ethernet transceiver is compliant with 10/100BASE-TX Ethernet standards, such as IEEE802.3/802.3u and ANSI X3.263-1995, and MAC protocol refers to an IEEE standard 802.3-2000.

4.9.1 Features:

- 10/100 Mbps data transfer.
- Conforms to IEEE 802.3-2002 specification.
- Supports full-duplex and half-duplex modes.
  - Supports CSMA/CD protocol for half-duplex operation.
  - Supports IEEE802.3x flow control for full-duplex operation.
- Programmable MAC address.
- CRC-32 algorithm calculates the FCS nibble at a time, automatic FCS generation and checking, able to capture frames with CRC errors if required.
- Promiscuous mode support.
- Station Management (STA) entity included.
- Supports double buffering for 2kB TX and 2kB RX memory.
- Two LED indicators used by Ethernet multi-function.

4.10 CAN Bus Controller

The FT90x series contains two CAN controllers, CAN bus 0 and CAN bus 1. Controller Area Network (CAN) is a high performance communication protocol for serial data communication. It is widely used in automotive and industrial applications. However this is expanding due to its reliability and feasibility. CAN bus uses a multi-master bus scheme with one logic bus line and equal nodes. The number of nodes is not limited by the protocol. Nodes do not have specific addresses. Instead, message identifiers are used, indicating the message content and priority of the message. FT900 CAN bus supports multicasting and broadcasting with an external CAN transceiver.

4.10.1 Features:

- Conforms to protocol version 2.0 parts A and B.
- Supports bit rates of up to 1 Mbit/s.
- Supports standard (11-bit identifier) and extended (29-bit identifier) frames.
- Support hardware message filtering with dual/single filters.
- 64 Bytes receiver and 16 Bytes transmitter FIFO.
- No overload frames are generated.
- Supports normal and listen-only modes.
- Supports single shot transmission.
- Supports an abort transmission feature.
- Readable error counters and last error code capture supported.

4.11 Real Time Clock

The Real Time Clock (RTC) is a set of counters for measuring time when system power is on, and the internal regulator will provide power to the RTC. It is clocked by a 32.768 kHz oscillator.

4.11.1 Features:

- No need external battery power supply.
- Alarm interrupt can be generated for a specific data/time setting.
- Hardware reset does not interrupt the RTC counter.

4.12 One-Wire Debugger Interface

The Debugger interface provides the capability, over a One-Wire half duplex serial link, to access memory mapped address space, such as the FT900 Flash memory, program memory, data memory and I/O memory. However, there is no transfer capability from any of the internal memory to the debugger interface.

4.12.1 Features:

- Single wire half duplex link that has one Start, eight Data and one Stop bits at a 1M bit/s rate.
- Supports debugger command read / write operation with variable data transfer.
- Supports CHIP ID read out.
- Supports checksum check by Flash memory operation.
- Supports CPU software debugging to execute Run, Stop, Step, Halt, Set software breakpoint, etc. operations.
- Use semaphore flag to control resource allocated by CPU or Debugger.

4.13 SPI Interface

The FT90x series contains an SPI master and SPI0, SPI1 slave controllers. SPI is a full duplex serial interface designed to handle multiple masters and slaves connected to a given bus.

4.13.1 Features:

- Maximum SPI data bit rate 25MHz in master and slave modes.
- Full duplex synchronous serial data transfer.
- Compliant with SPI specification, support four transfer formats.
- SPI master supports Single, Dual and Quad SPI transfer.
- SPI0, SPI1 slave support Single transfer only.

- Support SPI mode and FIFO mode operations.
- Multi-master system supported.
- Support bus error detection.
- SPI master can address up to 4 SPI slave devices.
- Support 64 Bytes receiver and 64 Bytes transmitter FIFO respectively.

4.14 I²C Interface

The FT90x series supports an I²C bus controller which is a bidirectional two wire interface. The two wires are Serial Clock line (SCL) and Serial Data line (SDA). The interface can be programed to operate with arbitration and clock synchronization allowing it to operate in multi-master systems. I²C0 and I²C1 support transmission speed up to 3.4Mb/s.

4.14.1 Features:

- Conforms to v2.1 and v3.0 of the I²C specification.
  - UM10204 I²C-bus specification and user manual Rev. 6 – 4 April 2014
- Support flexible transmission speed modes:
  - Standard (up to 100 kb/s)
  - Fast (up to 400 kb/s)
  - Fast-plus (up to 1 Mb/s)
  - High-speed (up to 3.4 Mb/s)
- I²C0 and I²C1 can be configured for Master or Slave mode.
- Perform arbitration and clock synchronization.
- Multi-master systems supported.
- Support both 7-bit and 10-bit addressing modes on the I²C bus.
- Support clock stretching.

4.15 UART Interface

The FT90x series contains two UART controllers with standard transmit and receive data lines. UART0 provides a full modem control handshake interface and support for 9-bit data, allowing automatic address detection while 9-bit data mode is enabled.

UART1 is a simplified programmable serial interface with CTS and RTS flow control logic. The signals are multiplexed with UART0 and can only be used if UART0 is used in simple mode (CTS/RTS only).

4.15.1 Features:

- Maximum UART data bit rate of 8 Mbit/s.
- Support UART mode and FIFO mode operation.
- 128 Bytes buffering both Receive and Transmit FIFOs used.
- Software compatible with 16450, 16550, 16750 and 16950 industry standard.
- Modem control function (CTS, RTS, DSR, DTR, RI, and DCD) support for UART0.
- Programmable automatic out-of- band flow control logic through Auto-RTS and Auto-CTS.
- Programmable automatic flow control logic using DTR and DSR.
- Programmable automatic in-band flow control logic using XON/XOFF characters.
- Support external RS-485 buffer enable.
- Fully programmable serial interface characteristics:
  - 5-, 6-, 7-, 8-, or 9-bit data characters
  - Even, Odd, or No-parity bit generation and detection
  - 1-, 1.5- or 2-stop bit generation
  - Baud rate generation

  - Detection of bad data in Receive FIFO
- Support Transmitter and Receiver disable capability.

4.16 Timers and Watchdog Timer

The FT90x series has four 16-bit user timers with pre-scaling and a 32-bit watchdog feature.

The watchdog timer is controlled from the main clock. The watchdog can be initialized with a 5-bit register. The value of this register points to a bit of the 32-bit counter which will be set by the application firmware. As the timer decrements, an interrupt occurs when the timer rolls over. Once started and initialized the watchdog can't be stopped. It can only be cleared by writing into a register.

The four user timers can be controlled from the main clock or a common 16-bit pre-scaler, which can be selected by each timer individually. These timers can be started, stopped and cleared / initialized. The current value of all timers can be read from registers. All timers can count up / down and signal an interrupt when the timer rolls over. The timers can also be configured to be one-shot or in continuous mode.

4.16.1 Features:

- Four user timers with pre-scaler.
- Supports 16-bit pre-scaler with system clock reference.
- Supports individual timer interrupt generated.
- Supports one-shot and continuous count for timer.
- Supports 32-bit counter watchdog.
- Supports watchdog interrupt generated.

4.17 I^2S Interface

The FT900 I^2S interface supports both Master and Slave modes. The formats supported are I^2S, Left Justified and Right Justified.

In Master mode, two clock sources are to be provided externally. One is 24.576MHz and the other is 22.5792MHz. The LRCLK, BCLK and MCLK as output signals will be generated by the Master based on sampling rate and data bit length.

In Slave mode, the LRCLK and BCLK are input signals to the FT900. The MCLK source is not used in this case. The application can configure the two clock source pins (I2SM_CLK22, I2SM_CLK24) to GPIO operation.

4.17.1 Features:

- Configure I^2S interface as master or slave.
- Support I^2S, Left Justified and Right Justified format.
- Support different sample rates: 11.025KHz, 22.05KHz, 44.1KHz, 16KHz, 32KHz, 48KHz, 96KHz and 192KHz.
- Support different audio data bit length: 16 bits, 20 bits, 24 bits and 32 bits.
- 2kB FIFO for I^2S receiver and 2kB FIFO for transfer audio data.
- Support FIFO flow control.
- Support master clock sources: 24.576MHz and 22.5792MHz.

4.18 Camera Parallel Interface (Data Capture)

The Camera Parallel Interface (CPI) implements an 8-bit parallel link from an image sensor to the FT900. The interface will provide a clock to the external camera module at a Max rate of 25MHz.

Camera control signals are VSYNC, HREF and PCLK. The VSYNC signal determines when a new frame begins. The HREF signal represents the period of data transfer of a row in the

transmitted frame. When the HREF signal is active, there is valid data over the data lines every pixel clock (PCLK) cycle. The PCLK signal indicates a valid data byte over the data lines and it is used as a transfer trigger.

4.18.1 Features:

- Configure camera registers via I^2C two-wire interface.
- 8-bit data is clocked by an external clock provided by the camera module.
- With VSYNC, HREF and PCLK control signals.
- Programmable data capture trigger position.
- 2kB FIFO for camera capture data.

4.19 PWM

The FT90x series supports 7 separate independent PWM output channels. All channels share an 8-bit pre-scaler to scale the system clock frequency to the desired channels.

Each channel has its own 16-bit comparator value. This is the value that would be matched to a preset 16-bit counter. When a channel's 16-bit comparator value matches that of the 16-bit counter, the corresponding PWM channel output will toggle. This 16-bit comparator value will continue to count until it reaches its preset value, and the counter will just roll over.

A special feature allows the 7 channels each to also toggle its own output based on the comparison results of other channels. Hence each channel potentially can have up to 8 toggle edges. The PWM signal generated can be output as a single-shot or continuous output.

The PWM counter also supports an external trigger. There are 6 GPIOs selectable for an external trigger.

PWM channel 0 and channel 1 can double as a stereo 11 KHz or 22 KHz PCM audio channel. Once this feature is setup, the 16-bit or 8-bit PCM audio data can be downloaded to the PWM local FIFO which can hold up to 64 bytes stereo or 128 bytes mono audio data. The data will playback based on the pre-scaler and 16-bit counter, and the data will be automatically scaled to fit in the playback period if necessary.

4.19.1 Features:

- Support 7 PWM output channels.
- Support single-shot or continuous PWM data output.
- Support external GPIO trigger.
- Support 16-bit / 8-bit stereo PCM audio data output.
- Control PCM FIFO full, empty, half-empty, overflow and underflow buffer management.
- Support PCM volume control for audio playback.

4.20 SD host controller

The FT90x series contains one SD host controller offering access to external large capacity non-volatile memory.

4.20.1 Features:

- Compliant with SD host controller standard specification, version 3.0.
- Supports both streaming and non-streaming data transfers.
- Compliant with SD physical layer specification, version 3.0.
- Supports configurable SD bus modes: 4-bit mode and 8-bit mode.
- Compliant with SDIO card specification, version 2.0.
- Support 4K SRAM for data FIFO.
- Supports configurable 1-bit/4-bit SD card bus.
- Configurable CPRM function for security.
- Built-in generation and check for 7-bit and 16-bit CRC data.

- Card detection (Insertion/Removal).
- Supports read wait mechanism for SDIO function.
- Supports suspend/resume mechanism for SDIO function.

4.21 Analog to Digital Converter (ADC)

The FT90x series has a low-power, high-speed, successive approximation Analog-to-Digital Converter (ADC) that supports a 10-bit resolution and superior maximum sampling frequencies of up to 1 Mega Samples Per-second (MSPS). This ADC accepts analog inputs ranging from the ground supplies to the power supplies. This ADC can be used in various low-power and medium-resolution applications.

4.21.1 Features:

- 10-bit successive approximation ADC.
- Supports 7 channel input.
- Individual channels can be selected for conversion.
- Power-down mode support.
- Max conversion rate up to 1MSPS.
- Measurement range 0 to VCC3V3A, by default the range voltage is 10% off of VCC3V3A. See Table 5-7.
- INL: 0.56/-1.05 LSB (Typ.).
- DNL: 0.66/-0.58 LSB (Typ.).

4.22 Digital to Analog Converter (DAC)

The FT90x series has two 10-bit, 1 Mega Samples Per-second (MSPS) Digital-Analog converter (DAC). It includes digital logic for registering the DAC value and a unity-gain buffer capable of driving off-chip. The module can also be switched to a power-down state where it consumes a minimum amount of current. The maximum output value of the DAC is DAC_REFP.

4.22.1 Features:

- Two 10-bit DACs (0/1).
- 10-bit R-2R DAC ladder structure.
- Buffered output.
- Power-down mode support.
- Programmable conversion rate, the maximum rate is 1MHz.
- Selectable output drive.

4.23 General Purpose Input Output

The FT90x series provides up to 65 configurable Input / Output pins controlled by GPIO registers. All pins have multiple functions with special peripheral connection. Separate registers allow setting or clearing any number of outputs simultaneously. All GPIO pins default to inputs with pull-down resistors enabled on reset except GPIO0/1/2 inputs that have pull-up resistors enabled.

All GPIOs can function as an interrupt. The polarity can be either positive edge or negative edge if its interrupt capability is enabled. In this case, the GPIO pin must be configured as a GPIO input.

4.23.1 Features:

- All GPIO default to inputs after reset (except GPIO0/1/2).
- Multi-function selection on GPIO pins.

- Pull-up/Pull-down resistor configuration and open-drain configuration can be programmed through the pin connect block for each GPIO pin.
- Direction control of individual bits.
- Supports GPIO input Schmitt trigger to help remove noise.
- Supports GPIO interrupt, where each enabled GPIO interrupt can be used to wake-up the system from power-down mode.

4.24 System Clocks

4.24.1 12 MHz Oscillator

The oscillator generates a 12 MHz reference frequency output to the clock multiplier PLL. The oscillator clock source comes from either an external 12 MHz crystal or a 12 MHz square wave clock. The external crystal is connected across XI/CLKIN and XIO in the configuration shown in Section 6.1. The optional external clock input is connected to XI/CLKIN only.

4.24.2 Phase Locked Loop

The internal PLL takes a 12 MHz clock input from a crystal oscillator. The PLL outputs the 100 MHz system clock frequency to the CPU processor and other peripheral circuits. Each peripheral has an individual enable control signal to gate the clock source.

4.24.3 32.768 KHz RTC Oscillator

The RTC oscillator provides a clock to the RTC time counter. Either an external 32.768 kHz crystal or a 32.768 kHz square wave clock can be used as the clock source. The external crystal is connected across RTC_XI/RTC_CLKIN and RTC_XIO in the configuration shown in Section 6.2. The optional external clock input is connected to RTC_XI/RTC_CLKIN only.

4.24.4 Internal Slow Clock Oscillator

The internal slow clock oscillator provides at least 5ms slow clock source to generate an interrupt for the USB2.0 device remote wake-up feature. A USB2.0 device with remote wake-up capability may not generate resume signalling unless the bus has been continuously in the idle state for 5ms. The detail description for USB2.0 suspend/resume, please refer to USB2.0 specification chapter7.1.7.7.

4.25 Power Management

4.25.1 Power Supply

The FT90x series may be operated with a single supply of +3.3V applied to VCCIO3V3, VUSB3V3, VETH3V3 and VCC3V3A pins. The +1.2V internal regulator VOUT1 provides the power to the core circuit after VCCIO3V3 power on and the system will generate a Power on Reset (POR) pulse when the output voltage rises above the POR threshold.

The second +1.2V internal regulator VOUT2 will provide the power to the Ethernet transceiver when VETH3V3 gets the power supply.

4.25.2 Power Down Mode

Power down mode applies to the entire system. In the power down mode, the system 12MHz oscillator and PLL both switch off and the system clock to the core and all peripherals stop except for the RTC oscillator and internal regulator. The internal regulator retains the power for the core and RTC running.

An interrupt from GPIO or wake-up events from the USB2.0 peripheral controller and host controller can wake-up the system from the power down mode independently.

If the USB2.0 host controller was used and the respective interrupt bit enabled before the system entered into power down mode, then the following events can wake-up the system.

- Remote wake-up interrupt to USB2.0 host controller.
- USB device connected interrupt to USB2.0 host controller.
- USB device disconnected interrupt to USB2.0 host controller.
- USB host controller detected the over-current (OC) protection event.

If the USB2.0 peripheral controller was used and the respective interrupt bit was also enabled before the system entered into power down mode, then the following events can wake-up the system.

- USB2.0 peripheral controller detects connect interrupt.
- USB2.0 peripheral controller detects disconnect interrupt.
- USB host issue reset signal to USB2.0 peripheral controller.
- USB host issue resume signal to USB2.0 peripheral controller.

5 Devices Characteristics and Ratings

5.1 Absolute Maximum Ratings

The absolute maximum ratings for the FT900 series devices are as follows. These are in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these may cause permanent damage to the device.

Parameter	Value	Unit
Storage Temperature	-65 to +150	°C
Floor Life (Out of Bag) At Factory Ambient (30°C / 60% Relative Humidity)	168 Hours (IPC/JEDEC J-STD-033A MSL Level 3 Compliant)*	Hours
Ambient Temperature (Power Applied)	-40 to +85	°C
VCC3V3 Supply Voltage	-0.5 to +4.6	V
DC Input Voltage – Host H_DP and H_DM	-0.5 to +5	V
DC Input Voltage – Peripheral D_DP and D_DM	-0.5 to +5	V
DC Input Voltage – Ethernet TXON, TXOP, RXIN and RXIP	-0.5 to +5.6	V
DC Input Voltage – 5V tolerance I/O cells	-0.5 to +5.8	V
Others (ADC, DAC) – 3V I/O cells	-0.5 to VCC3V3+0.5	V

Table 5-1 Absolute Maximum Ratings

* If devices are stored out of the packaging beyond this time limit the devices should be baked before use. The devices should be ramped up to a temperature of +125°C and baked for up to 17 hours.

5.2 DC Characteristics

Electrical Characteristics (Ambient Temperature = -40°C to +85°C)

The typical values are obtained at room temperature (T_j = 25°C), VCC3V3 = 3.3V, and VCC1V2 = 1.2V.

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
VCCIO3V3	I/O operating supply voltage	2.97	3.3	3.63	V	Normal Operation
I_{cc1}	Power down current	-	700	-	uA	Power Down Mode
I_{cc2}	Idle current	-	42	-	mA	Idle
I_{cc3}	System operating current*	-	75	-	mA	USB2.0 Host controller high speed transfer data
		-	75	-	mA	USB2.0 Peripheral controller high speed transfer data
		-	100	-	mA	10/100 Mbit/s Ethernet transfer data
		-	50	-	mA	ADC / DAC Operation
VOUT1	Internal LDO voltage	-	1.2	-	V	Normal Operation

Table 5-2 Operating Voltage and Current

Note*: The system operating typical current measured based on each function implements normal operation with FT32 core active, and other peripherals keep idle status.

DC characteristics of I/O cells

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
V_{oh}	Output Voltage High	2.4	-	-	V	$\|I_{oh}\|$=2mA~16mA
V_{ol}	Output Voltage Low	-	-	0.4	V	$\|I_{ol}\|$=2mA~16mA
V_{opu}*	Output pull-up Voltage for 5V tolerance I/Os	VCCIO3V 3-0.9	-	-	V	$\|I_{pu}\|$ = 1uA
V_{ih}	Input High Voltage	2.0	-	-	V	LVTTL
V_{il}	Input Low Voltage	-	-	0.8	V	LVTTL
V_{th}	Schmitt trigger positive threshold Voltage	-	1.6	2.0	V	LVTTL

V_{tl}	Schmitt-trigger negative threshold Voltage	0.8	1.1	-	V	LVTTL
R_{pu}	Input pull-up resistance equivalent	40	75	190	KΩ	V_{in} = 0V
R_{pd}	Input pull-down resistance equivalent	40	75	190	KΩ	V_{in} = VCCIO3V3
I_{in}	Input leakage current	-10	±1	+10	uA	V_{in} = VCCIO3V3 or 0
C_{in}*	Input Capacitance	-	2.8	-	pF	VCCIO3V3 with 5V tolerance I/O

Table 5-3 Digital I/O Pin Characteristics (VCCIO3V3 = +3.3V, Standard Drive Level)

Note*: This parameter indicates that the pull-up resistor for the 5V tolerance I/O cells cannot reach VCCIO3V3 DC level even without DC loading current.

C_{in} includes the cell layout capacitance and pad capacitance.

DC characteristics of USB I/O cells

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
General characteristics						
VUSB3V3	USB power supply voltage	2.97	3.3	3.63	V	Normal operation
VCC1V2*	USB core supply voltage	1.08	1.2	1.32	V	Normal operation
Input level for high speed						
V_{hscm}	Voltage of high speed data signal in the common mode	-50	-	500	mV	-
V_{hssq}	High speed squelch detection threshold	-	-	100	mV	Squelch is detected
		150	-	-	mV	Squelch is not detected
V_{hsdsc}	High speed disconnection detection threshold	625	-	-	mV	Disconnection is detected
		-	-	525	mV	Disconnection is not detected
Output level for high speed						
V_{hsoi}	High speed idle output voltage (Differential)	-10	-	10	mV	-
V_{hsol}	High speed low level output voltage (Differential)	-10	-	10	mV	-
V_{hsoh}	High speed high level output voltage	-360	-	400	mV	-

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
	(Differential)					
V_{chirpj}	Chirp-J output voltage (Differential)	700	-	1100	mV	-
V_{chirpk}	Chirp-K output voltage (Differential)	-900	-	-500	mV	-
Input level for full speed and low speed						
V_{di}	Differential input voltage sensitivity	0.2	-	-	V	$\|V_{dp}-V_{dm}\|$
V_{cm}	Differential common mode voltage	0.8	-	2.5	V	-
V_{se}	Single ended receiver threshold	0.8	-	2.0	V	-
Output level for full speed and low speed						
V_{ol}	Low level output voltage	0	-	0.3	V	-
V_{oh}	High level output voltage	2.8	-	3.6	V	-
Resistance						
R_{drv}	Driver output impedance	40.5	45	49.5	ohm	Equivalent resistance used as an internal chip

Table 5-4 USB I/O Pin (D_DP/D_DM, H_DP/H_DM) Characteristics

Note*: The VCC1V2 is USB Host or Peripheral transceiver core power supply input which need connect to external +1.2V voltage power while USB Host or Peripheral controller is active.

DC characteristics of Ethernet I/O cells

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
General characteristics						
VETH3V3	Ethernet power supply voltage	2.97	3.3	3.63	V	Normal operation
VOUT2*	Ethernet LDO voltage	-	1.2	-	V	Normal operation
Total dissipative power	10Base-TX mode (Including TX current)	-	-	510	mW	10Base-TX mode
	10Base-TX mode (Excluding TX current)	-	-	147	mW	10Base-TX mode
	100Base-TX mode	-	-	310	mW	100Base-TX mode

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
	(Including TX current)					
	100Base-TX mode (Excluding TX current)	-	-	165	mW	100Base-TX mode
	Auto-negotiation mode (Including TX current)	-	-	550	mW	100Base-TX mode
	Auto-negotiation mode (Excluding TX current)	-	-	187	mW	100Base-TX mode
	Power down mode	-	-	10	mW	Ethernet power down

Table 5-5 Ethernet I/O pin (TXON/TXOP, RXIN/RXIP) characteristics

Note*: The VOUT2 is the internal Regulator +1.2V voltage output which provides a power supply for the internal Ethernet transceiver.

DC characteristics of DAC I/O cells

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
VCC3V3A	DAC power supply voltage	2.97	3.3	3.63	V	Normal Operation
VREFP	Reference voltage	0	-	VCC3V3A	V	DCAP_REFP positive reference
RES	Resolution	10	-	-	Bits	-
INL	Integral nonlinearity error	-2	-	2	LSB	VREFP = VCC3V3A
DNL	Differential nonlinearity error	-1	-	1.5	LSB	VREFP = VCC3V3A
-	Conversion latency	-	-	1	Clock cycle	-
C_{LOAD}	Output load: rated capacitance	-	-	10	pF	-
R_{LOAD}	Output load: rated resistance	6.7	-	-	KΩ	-

Table 5-6 DAC I/O pin (DAC_REFP, DAC0/1) characteristics

DC characteristics of ADC I/O cells

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
VCC3V3A	Analog power supply voltage	2.97	3.3	3.63	V	Normal operation
XAIN	Analog input range	0	-	VCC3V3A	V	-
RES	Resolution	-	10	-	Bit	-
INL	Integral nonlinearity error	-3	0.56/-1.05	3	LSB	10%-90% of VCC3V3A Reference
		-4	0.56/-1.05	4	LSB	Rail-to-Rail VCC3V3A reference
DNL	Differential nonlinearity error	-1	0.66/-0.58	1.75	LSB	-
Xsampleclk	Sample rate	-	-	1	MSPS	-

Table 5-7 ADC I/O Pin Characteristics

DC characteristics EFUSE cells

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
EFUSE Program Mode						
V_{DD}	Operating voltage	1.08	1.2	1.32	V	-
$V_{FSOURCE}$	FSOURCE voltage	3.6	3.7	3.8	V	-
V_{PP}	VPP voltage	1.8	1.85	1.9	V	-
I_{VPP}	VPP current	-	-	3	mA	-

Table 5-8 EFUSE I/O Pin Characteristics

5.3 AC Characteristics

AC Characteristics (Ambient Temperature = -40°C to +85°C)

System clock dynamic characteristics

Parameter	Value			Unit
	Minimum	Typical	Maximum	
Crystal oscillator				
Clock frequency	-	12.00	-	MHz
External clock input				
external clock jitter	-	-	500	ps
clock duty cycle	45	50	55	%
Input voltage on pin XI/CLKIN	-	3.3	-	V

Table 5-9 System clock characteristics

Note: Recommended accuracy of the clock frequency is 50ppm for the crystal.

RTC clock dynamic characteristics

Parameter	Value			Unit
	Minimum	Typical	Maximum	
Crystal oscillator				
Clock frequency	-	32768	-	Hz
External clock input				
external clock jitter	-	-	500	ps
clock duty cycle	45	50	55	%
Startup time	-	0.5	5	s
Input voltage on pin RTC_XI/RTC_CLKIN	-	1.2	-	V

Table 5-10 RTC clock characteristics

Analog USB I/O pins dynamic characteristics

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Driver characteristic for high speed						
T_{hsr}	High speed differential rise time	500	-	-	ps	-
T_{hsf}	High speed differential fall time	500	-	-	ps	-
Driver characteristic for full speed						
T_{fr}	Rise time of DP/DM	4	-	20	ns	Cl=50pF 10%~90% of |Voh–Vol|
T_{ff}	Fall time of DP/DM	4	-	20	ns	Cl=50pF 10%~90% of |Voh–Vol|
T_{frma}	Differential rise/fall time matching	90	-	110	%	The first transition exclude from the idle mode
Driver characteristic for low speed						
T_{lr}	Rise time of DP/DM	75	-	300	ns	Cl=200pF~600pF 10%~90% of |Voh–Vol|
T_{lf}	Fall time of DP/DM	75	-	300	ns	Cl=200pF~600pF 10%~90% of |Voh–Vol|
T_{lrma}	Differential rise/fall time matching	80	-	125	%	The first transition exclude from the idle mode

Table 5-11 Analog I/O pins (D_DP/D_DM, H_DP/H_DM) characteristics

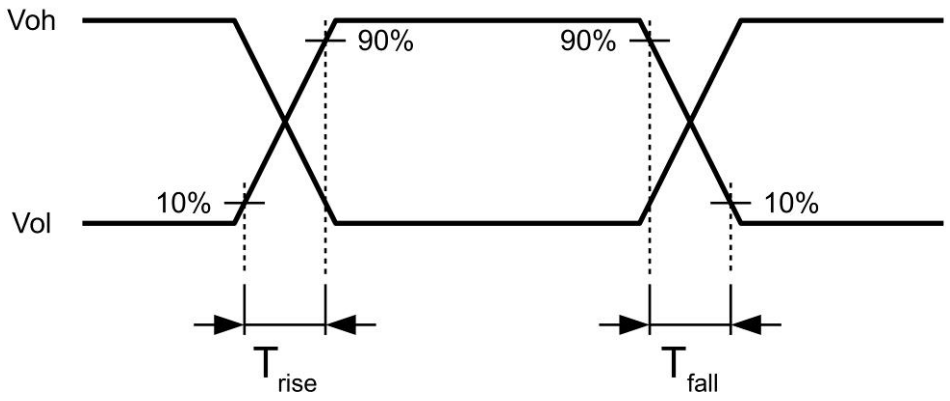


Figure 5-1 USB Rise and Fall Times for DP/DM

Analog Ethernet I/O pins dynamic characteristics

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Transmitter characteristics						
2 x V_{txa}	Peak-to-peak differential output voltage	1.9	2.0	2.1	V	100Base-TX mode
T_r / T_f	Signal rise/fall time	3.0	4.0	5.0	ns	100Base-TX mode
T_j	Output jitter	-	-	1.4	ns	100Base-TX mode, scrambled idle signal
V_{txov}	Overshoot	-	-	5.0	%	100Base-TX mode
Receiver characteristics						
-	Common-mode input voltage	2.97	3.3	3.63	V	-
-	Error-free cable length	100	-	-	meter	-

Table 5-12 Analog I/O pins (TXON/TXOP, RXIN/RXIP) characteristics

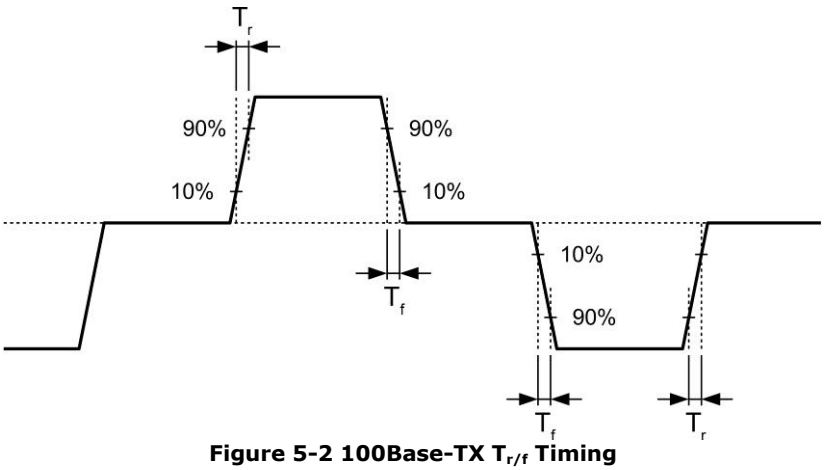


Figure 5-2 100Base-TX $T_{r/f}$ Timing

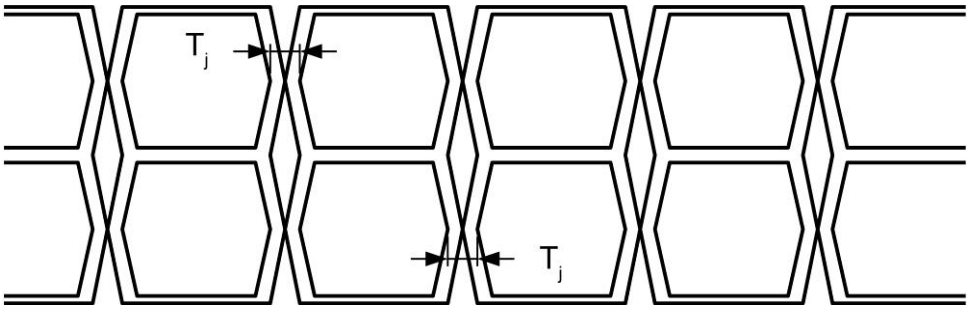


Figure 5-3 100Base-TX Jitter Timing

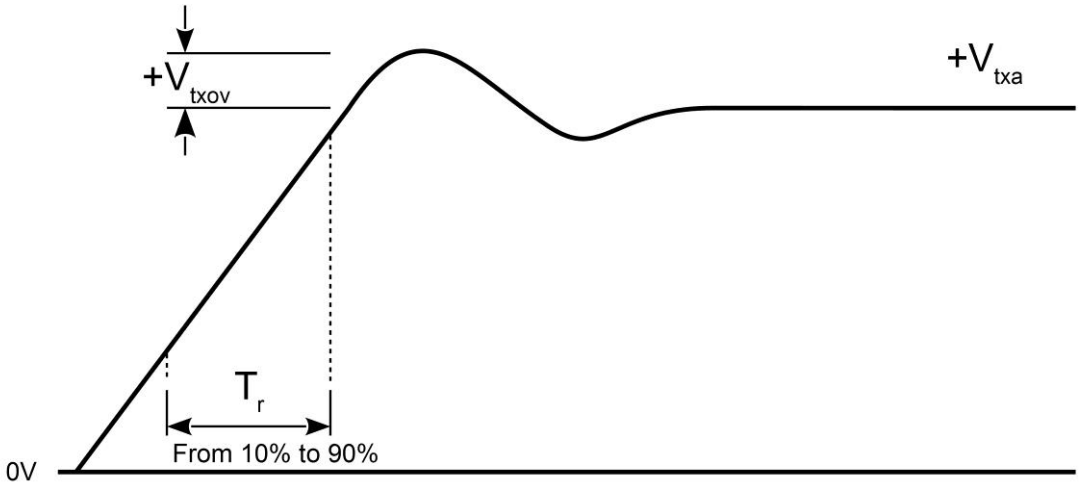


Figure 5-4 100Base-TX Transmission Waveform

I²C Bus I/O pins dynamic characteristics (V_{cc} (I/O) = 3.3V)

Parameter	Description	Standard mode (SM)		Fast mode (FM)		Fast mode Plus (FM+)		High Speed mode (HS)		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
F_{SCL}	SCL clock frequency	0	100	0	400	0	1000	0	3400	kHz
T_{SCLL}	SCL clock low period	4.7	-	1.3	-	0.5	-	0.320	-	µs
T_{SCLH}	SCL clock high period	4.0	-	0.6	-	0.26	-	0.120	-	µs
T_{SU}	data setup time	250	-	100	-	50	-	10	-	ns
T_{HD}	data hold time	0	-	0	-	0	-	0	150	ns
T_r	rise time	-	1000	-	300	-	120	20	160	ns
T_{rCL1}	rise time 1st clock after S_r (HS)							20	160	ns
T_{rCL}	rise time clock (HS)							20	80	ns
T_f	fall time	-	300	-	300	-	300	20	80 (SCL) 160 (SDA)	ns

Table 5-13 I2C I/O pins (I2C0_SCL/SDA, I2C1_SCL/SDA) characteristics

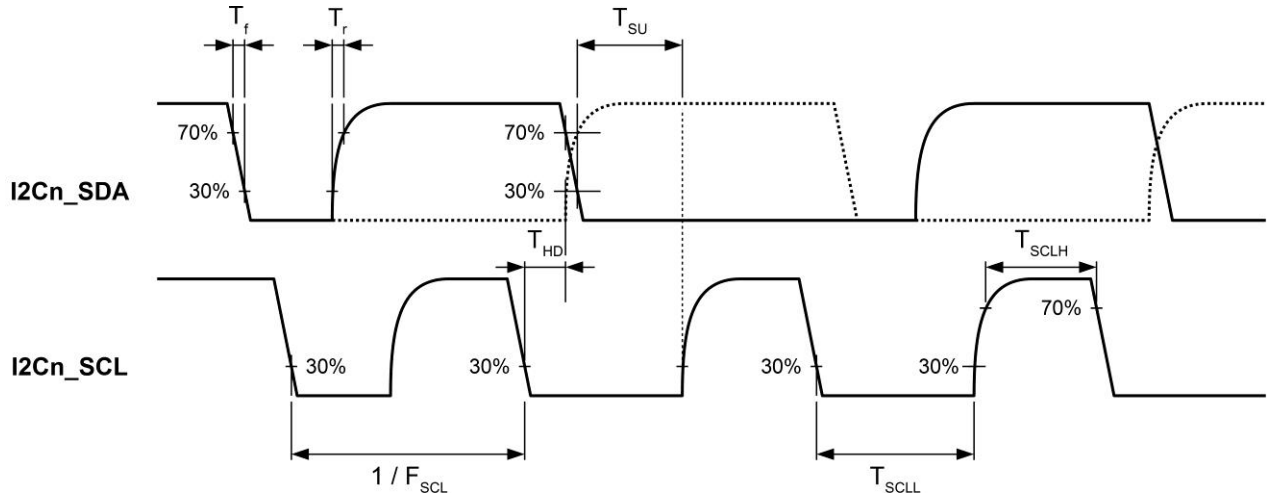


Figure 5-5 Definition of I²C Timing F/S mode

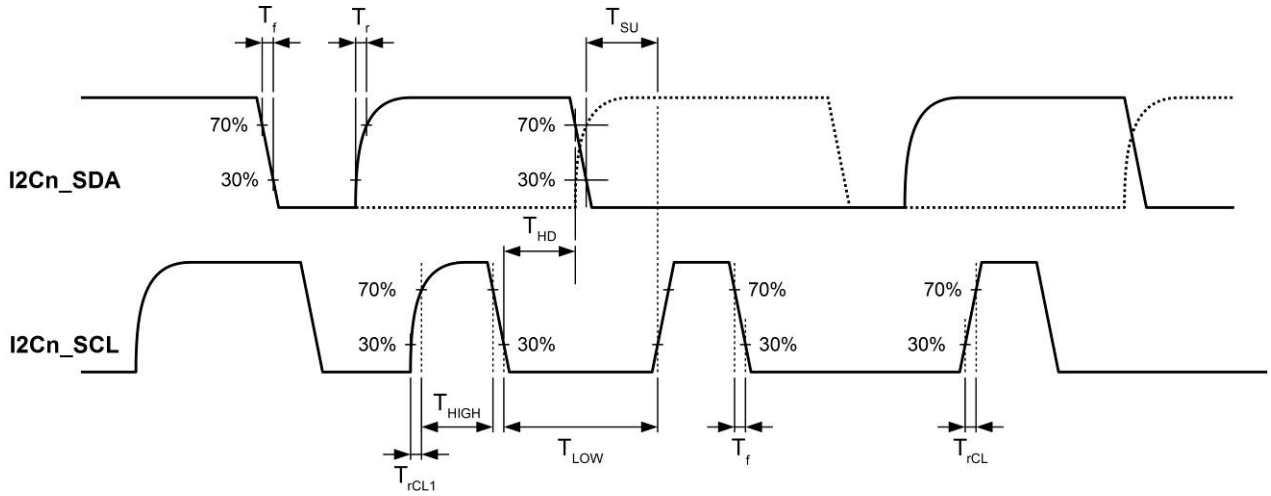


Figure 5-6 Definition of I²C Timing HS mode

SPI Master I/O pins dynamic characteristics (V_{cc} (I/O) = 3.3V)

Parameter	Description	V_{cc} (I/O) 3.3V			Unit
		Min	Typ	Max	
T_{SCLK}	SPI clock period	25			ns
T_{SCLKL}	SPI clock low duration	19			ns
T_{SCLKH}	SPI clock high duration	19			ns
T_{OD}	output data delay	19		20	ns

Table 5-14 SPI I/O pins (SPIM_CLK/MOSI/MISO/SS0/SS1/SS2/SS3) characteristics

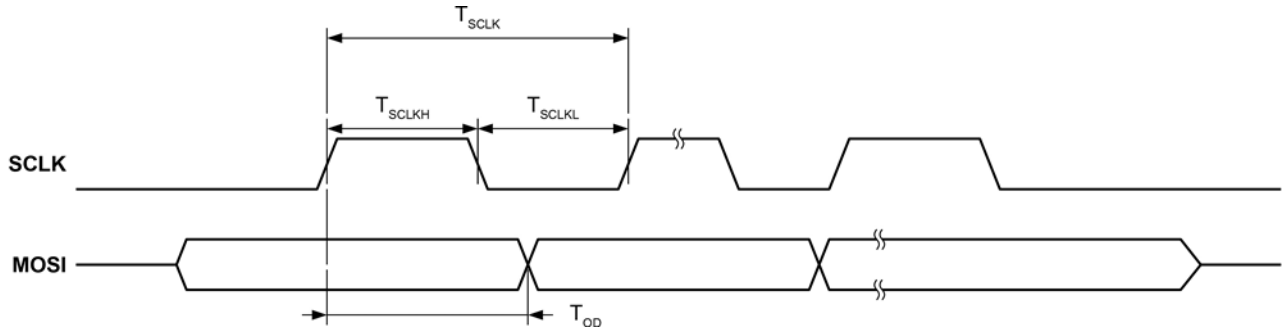


Figure 5-7 Definition of SPI Master Timing Mode 0

SPI Slave I/O pins dynamic characteristics (V_{cc} (I/O) = 3.3V)

Parameter	Description	V_{cc} (I/O) 3.3V			Unit
		Min	Typ	Max	
T_{SCLK}	SPI clock period	40			ns
T_{SCLKL}	SPI clock low duration	16			ns
T_{SCLKH}	SPI clock high duration	16			ns
T_{SAC}	SPI access time	20			ns
T_{OD}	output data delay	7		27	ns
T_{ZO}	output enable delay	10			ns
T_{OZ}	output disable delay	10			ns
T_{CSH}	CS hold time	0			ns

Table 5-15 SPI I/O pins (SPIS0_CLK/MOSI/MISO/SS, SPIS1_CLK/MOSI/MISO/SS) characteristics

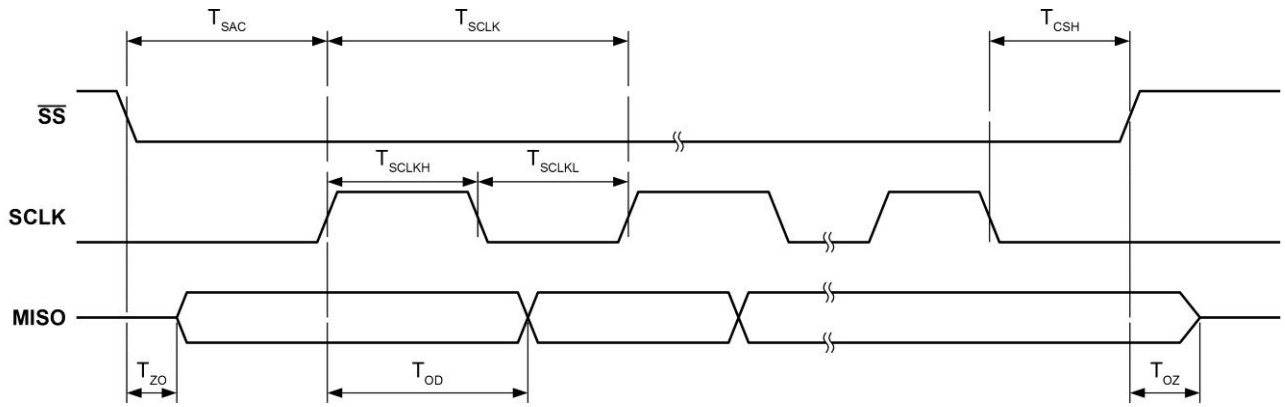


Figure 5-8 Definition of SPI Slave Timing Mode 0

I2S Master I/O pins dynamic characteristics (V_{cc} (I/O) = 3.3V)

Parameter	Description	Min	Typ	Max	Unit	Conditions
$T_{D(LRCLK)}$	LRCLK delay time	0		10	ns	fs = 48kHz BCLK = 256fs
$T_{D(SDAO)}$	SDAO delay time	0		15	ns	
$T_{SU(SDAI)}$	setup time	10			ns	
$T_{H(SDAI)}$	hold time	10			ns	

Table 5-16 I²S Master I/O pins (I2S_LRCLK/BCLK/SDAI/SDAO) characteristics

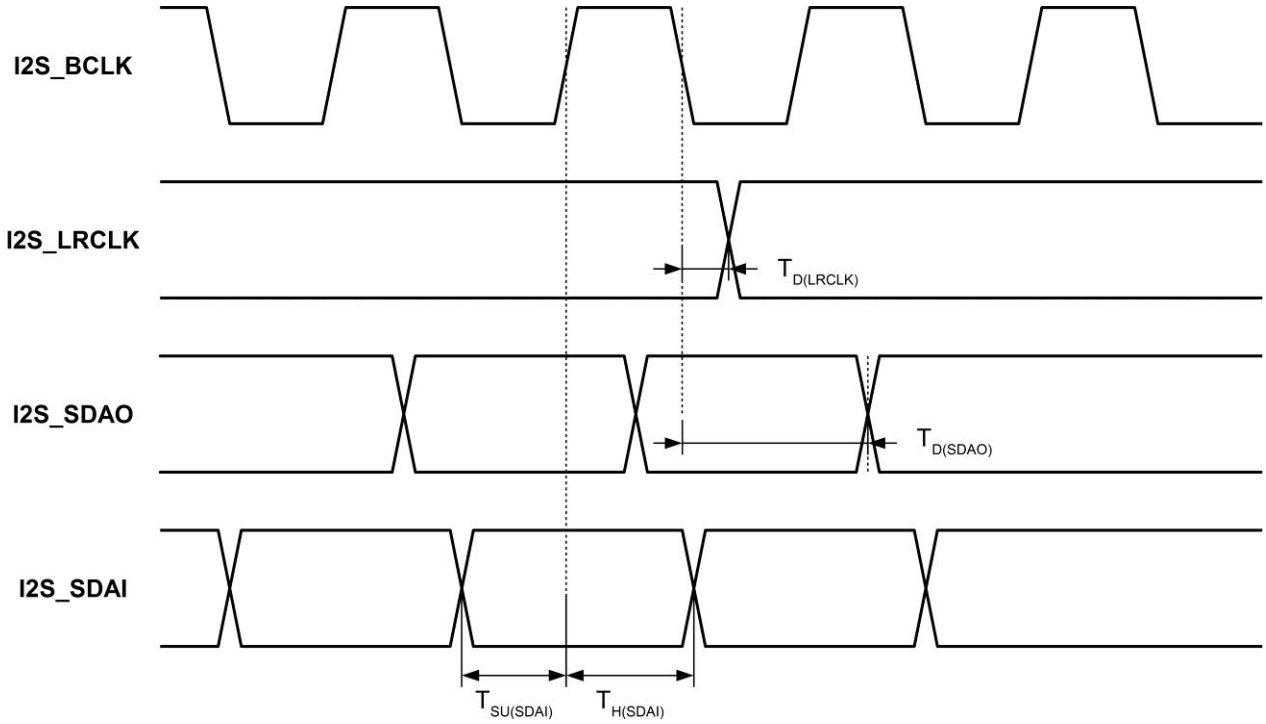


Figure 5-9 Definition of I²S Master Timing

I2S Slave I/O pins dynamic characteristics (V_{cc} (I/O) = 3.3V)

Parameter	Description	Min	Typ	Max	Units	Conditions
$T_{SU(LRCLK)}$	LRCLK setup time	10			ns	fs = 48kHz BCLK = 256fs
$T_{H(LRCLK)}$	LRCLK hold time	10			ns	
$T_{H(SDAO)}$	SDAO delay time	0		10	ns	
$T_{SU(SDAI)}$	SDAI setup time	10			ns	
$T_{H(SDAI)}$	SDAI hold time	10			ns	

Table 5-17 I²S Slave I/O pins (I2S_LRCLK/BCLK/SDAI/SDAO) characteristics

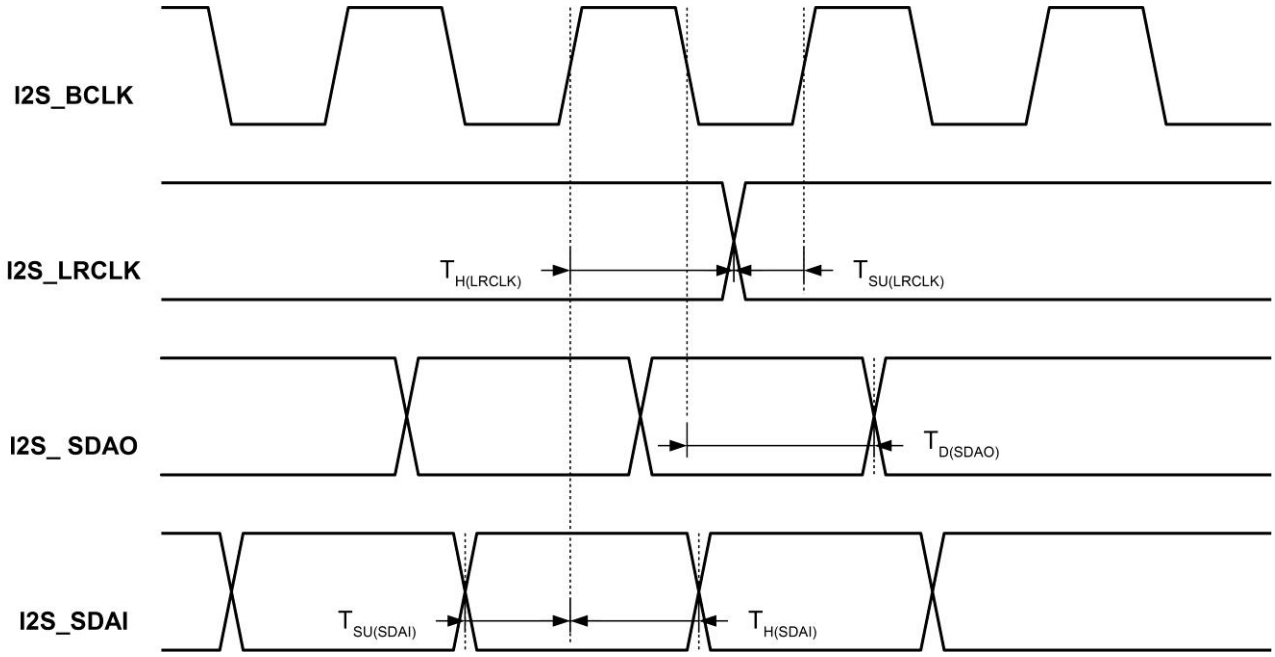


Figure 5-10 Definition of I²S Slave Timing

SD Host I/O pins dynamic characteristics (V_{cc} (I/O) = 3.3V)

Parameter	Description	Conditions	Min	Max	Unit
T_{SCLK}	clock period	on pin SD_CLK	40		ns
T_{ISU}	data input setup time		16		ns
T_{IH}	data input hold time		-2		ns
T_{ZO}	data output valid delay time			12	ns
T_{OZ}	data output hold time		0.3		ns

Table 5-18 SD Host I/O pins (SD_CLK, SD_CMD, SD_DATA3/DATA2/DATA1/DATA0, SD_CD, SD_WP) characteristics

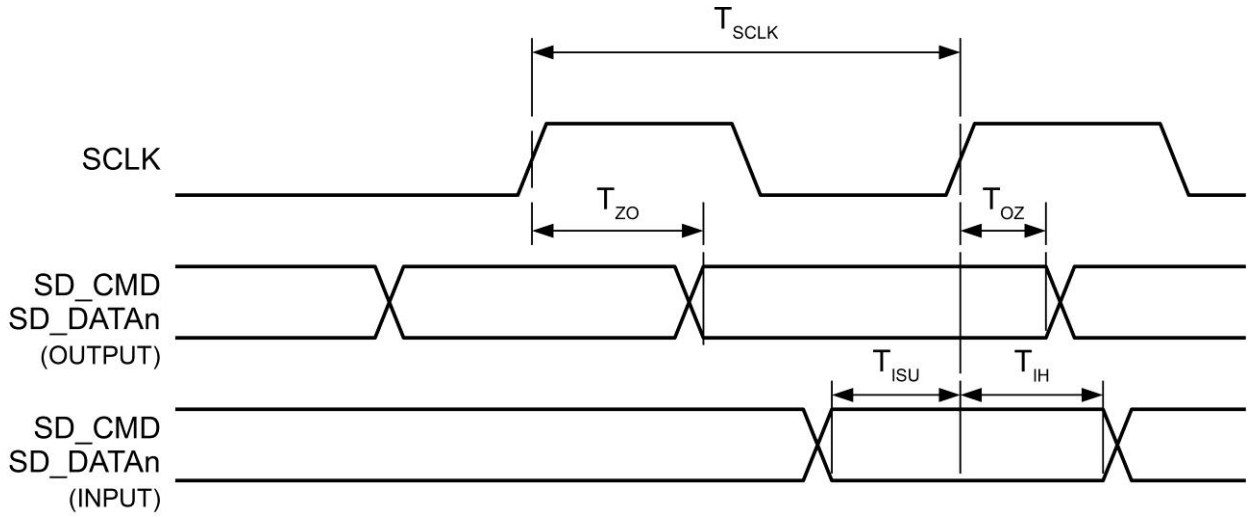


Figure 5-11 Definition of SD Host Timing

6 Application Information

6.1 Crystal Oscillator

The crystal oscillator operates at a frequency of 12MHz. The oscillator can operate one of two following configuration.

6.1.1 Crystal oscillator application circuit

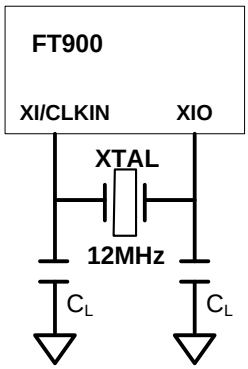


Figure 6-1 Crystal oscillator connection

Feedback resistance is integrated on chip, only a crystal and capacitors C_L need to be connected externally. With the proper selection of crystal, the oscillator circuit can generate better quality signals for FT900. Parameter C_L is typically 27pF but should be checked with the crystal manufacturer.

6.1.2 External clock input

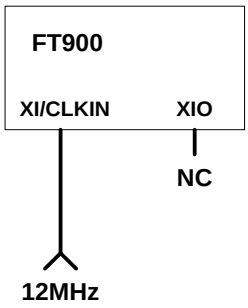


Figure 6-2 External clock input

The 12MHz input clock signal connects XI/CLKIN to internal oscillator directly. The XIO pin can be left unconnected.

6.2 RTC Oscillator

In the RTC oscillator circuit Figure 6-3, only a 32.768 KHz crystal and capacitors C_{RTCL} need to be connected externally. The parameter C_{RTCL} should be checked with the crystal manufacturer.

An external input clock Figure 6-4 can be connected to RTC_XI/RTC_CLKIN if RTC_XIO is left open.

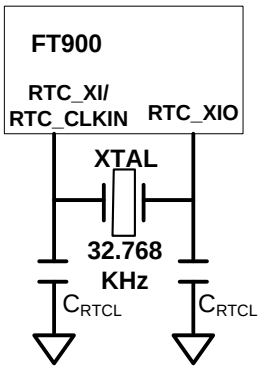


Figure 6-3 RTC 32.768 KHz oscillator connection

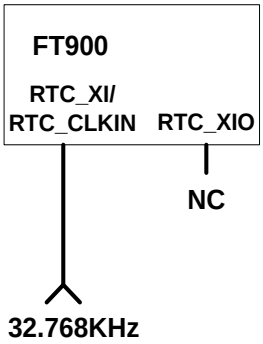


Figure 6-4 External 32.768 KHz clock input

6.3 Standard I/O Pin Configuration

Figure 6-5 shows the possible pin modes for standard I/O pins with multiplex functions:

- Output driver enabled
- Output driver capability control
- Output slew rate control
- Open drain output
- Input with pull-up enabled
- Input with pull-down enabled
- Input with keeper enabled
- Input with Schmitt trigger

The default configuration for standard I/O pins is input with pull-down enabled except GPIO 0/1/2. All I/O pins have ESD protection.

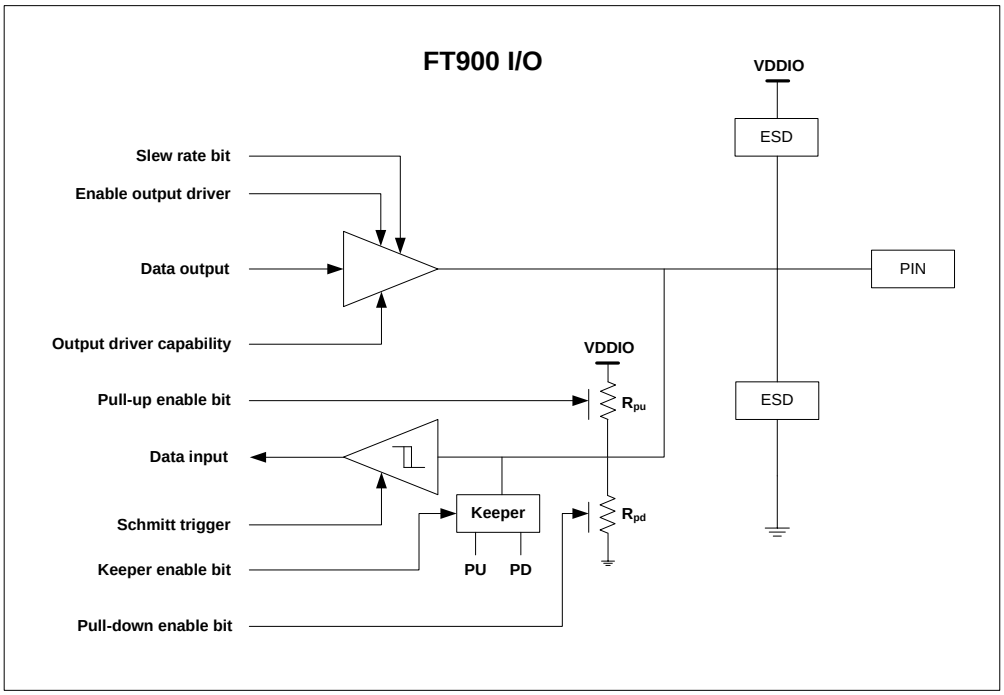


Figure 6-5 GPIO I/O ports connection

6.4 USB2.0 Peripheral and Host Interface

The example diagram in Figure 6-6 shows the FT90x series supporting one USB2.0 host port and one USB2.0 device port, which makes FT90x system data transfer easier via a USB adapter.

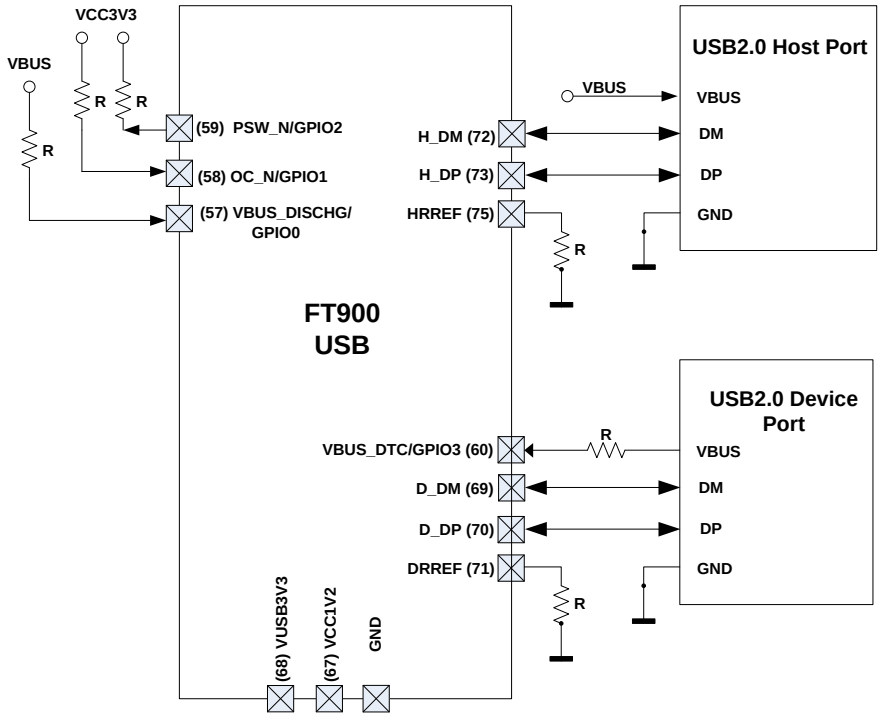


Figure 6-6 USB2.0 ports connection

The FT90x System shall provide I/O power (+3.3V supply) on VUSB3V3 and core power (+1.2V supply) on VCC1V2 for the USB2.0 peripheral / host controller. The internal band-gap gets a reference voltage from DRREF or HRREF with an external reference resistor R (12 KΩ ±1%) respective connected to GND.

The USB2.0 host control will provide a +5V power voltage output for VBUS and go through the PSW_N signal to control power switching on/off.

6.5 10/100 Mb/s Ethernet Interface

Figure 6-7 shows the 10/100 Mb/s Ethernet port configuration via the transmit (TXON & TXOP) and receive (RXIN & RXIP) differential pair pins.

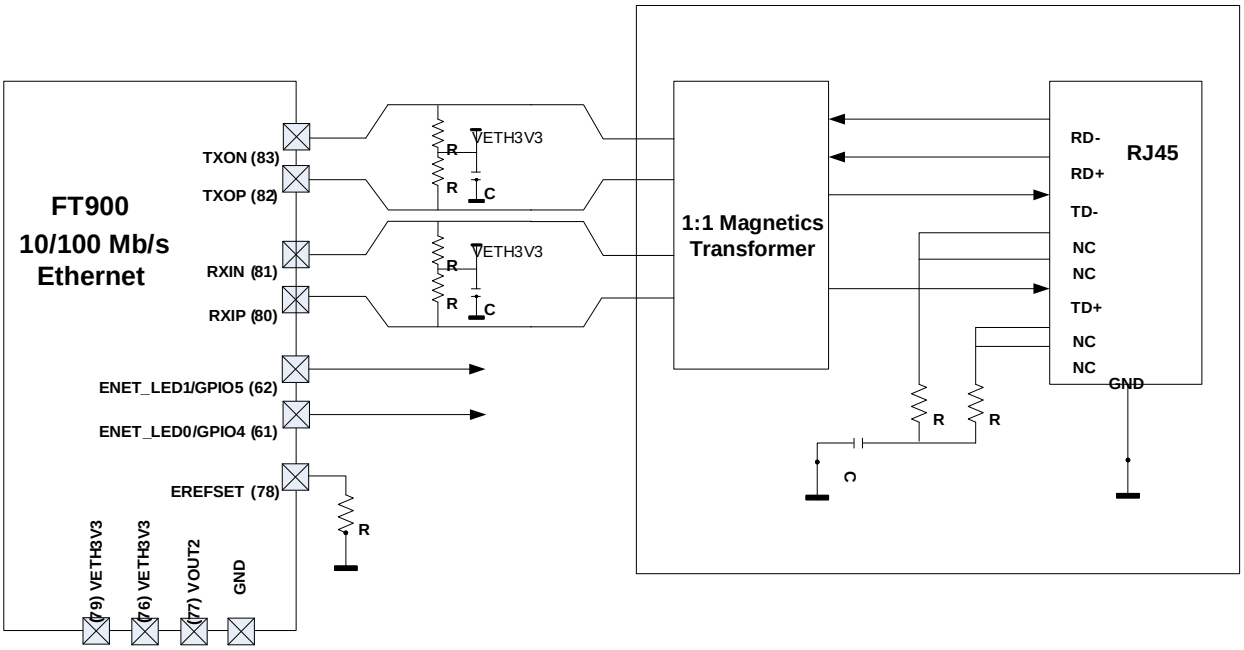


Figure 6-7 10/100Mbps Ethernet Interface

The FT90x Ethernet connection to a termination network should go through a 1:1 magnetics transformer and an RJ-45. For space saving, the magnetics and RJ-45 may be a single integrated component. The system shall provide +3.3V power supply for VETH3V3. The internal regulator will generate +1.2V output on VOUT2. The EREFSET connects an external resistor R (12 KΩ ±1%) to GND to provide a reference voltage for the Ethernet transceiver.

There are two Ethernet LEDs output for TX/RX transmission, Full-duplex/Half-duplex, Collision, Link or 10/100 Mb/s Speed indication. The required function should be set in the chip registers before using the LED indicator.

6.6 Ethernet Connection when Unused (FT900 & FT901)

If the Ethernet peripheral is not used in the end application, connect VETH3V3 to ground. See Figure 6-8 and Figure 6-9.

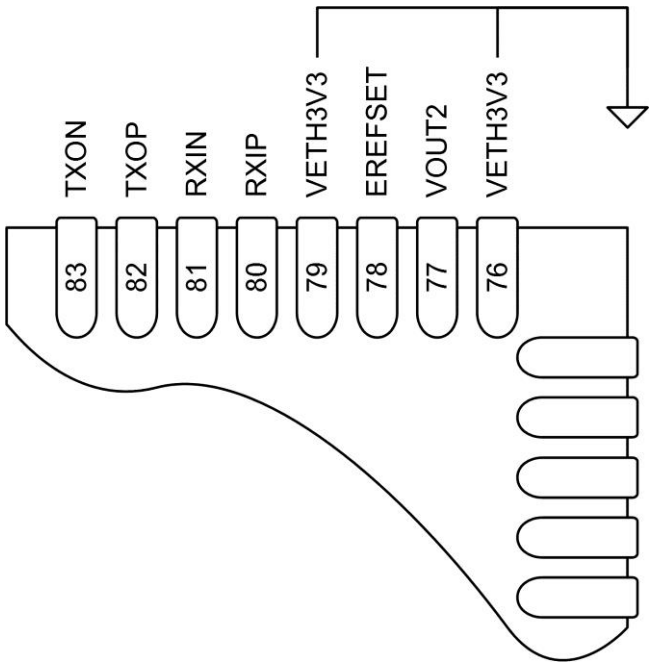


Figure 6-8 Unused Ethernet Connection (QFN)

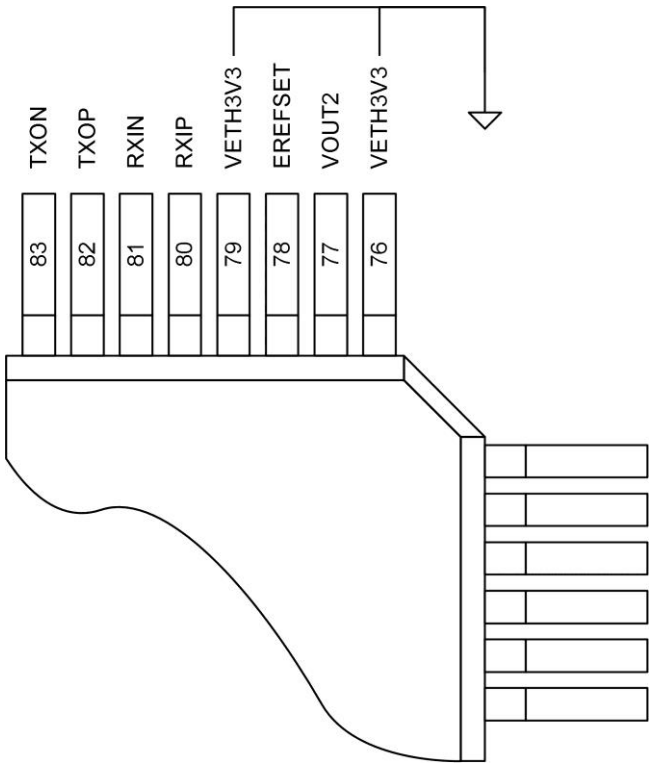


Figure 6-9 Unused Ethernet Connection (LQFP)

6.7 USB Connection when Unused (FT900_1_2_3)

If the USB peripheral (Host and Device) is not used in the end application, connect VUSB3V3, HRREF, and DRREF to ground. See Figure 6-10 and Figure 6-11.

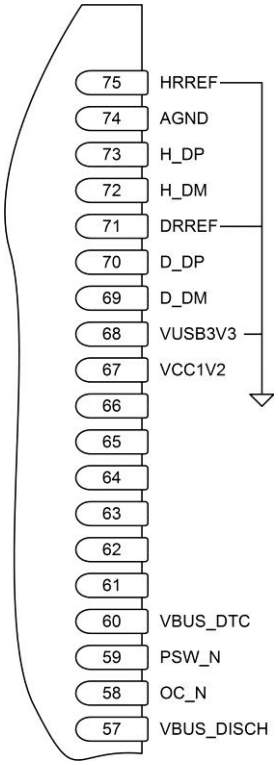


Figure 6-10 Unused USB Connection (QFN)

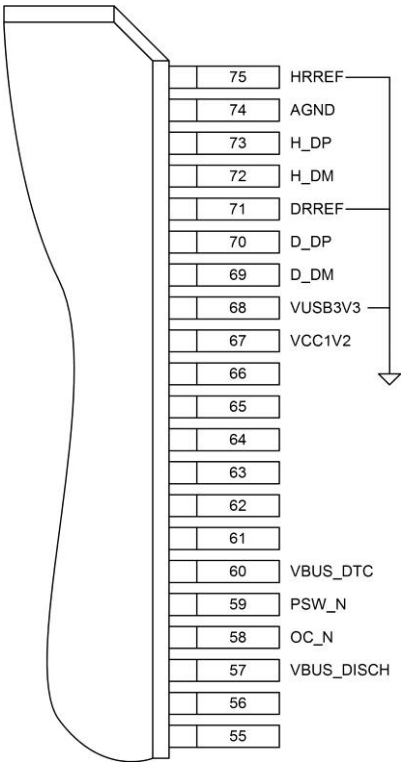
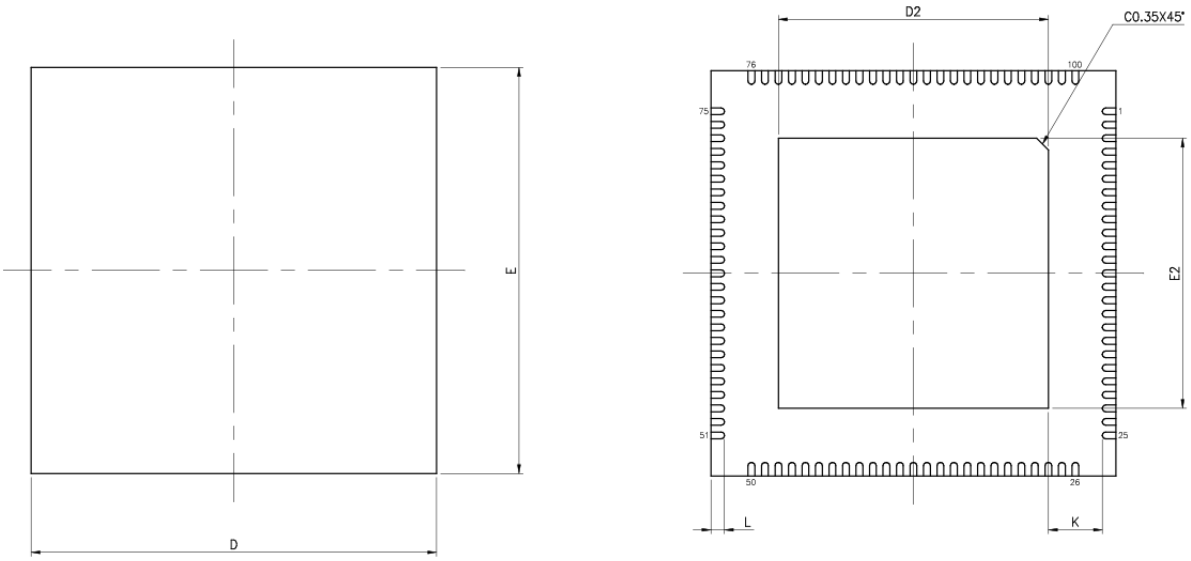


Figure 6-11 Unused USB Connection (LQFP)

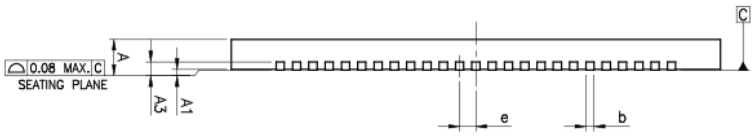
7 Package Parameters

The FT90x series is available in two different packages. The FT900Q/FT901Q/FT902Q/FT903Q are the QFN-100 package and the FT900L/FT901L/FT902L/FT903L are in the LQFP-100 package. The dimensions, markings and solder reflow profile for all packages are described in following sections.

7.1 QFN-100 Package Dimensions



SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203 REF.		
D	12.00 BSC		
E	12.00 BSC		
b	0.15	0.20	0.25
e	0.40 BSC		
L	0.35	0.40	0.45
K	0.20	—	—



UNIT : mm

PAD SIZE	D2			E2			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
	7.95	8.00	8.05	7.95	8.00	8.05	V	X	N/A

Figure 7-1 QFN-100 Package Dimensions

Note: On the underside of the package, the exposed thermal pad should be connected to GND.

7.2 QFN-100 Device Marking

7.2.1 FT90XQ Top Side

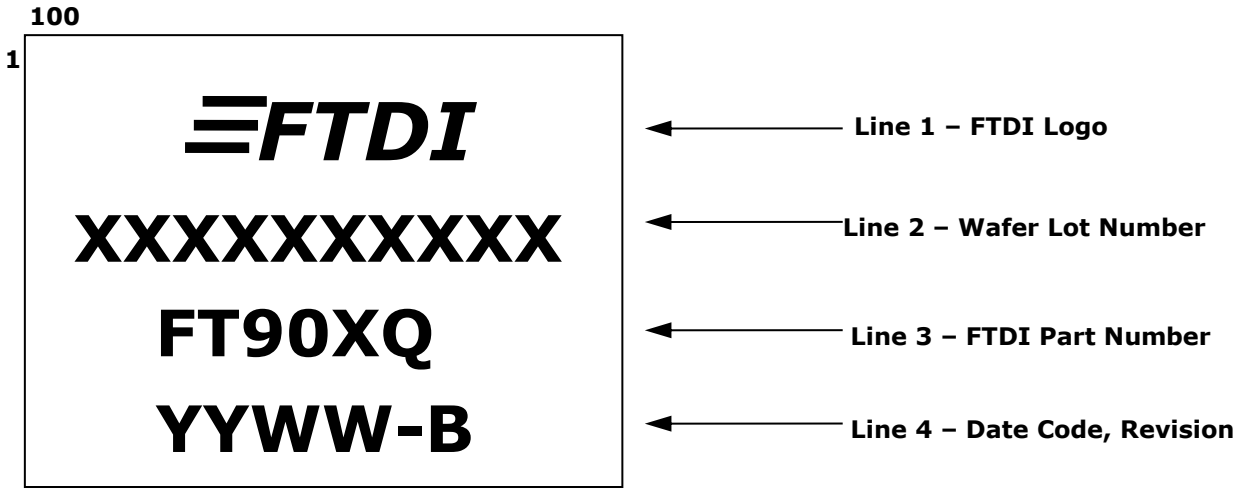


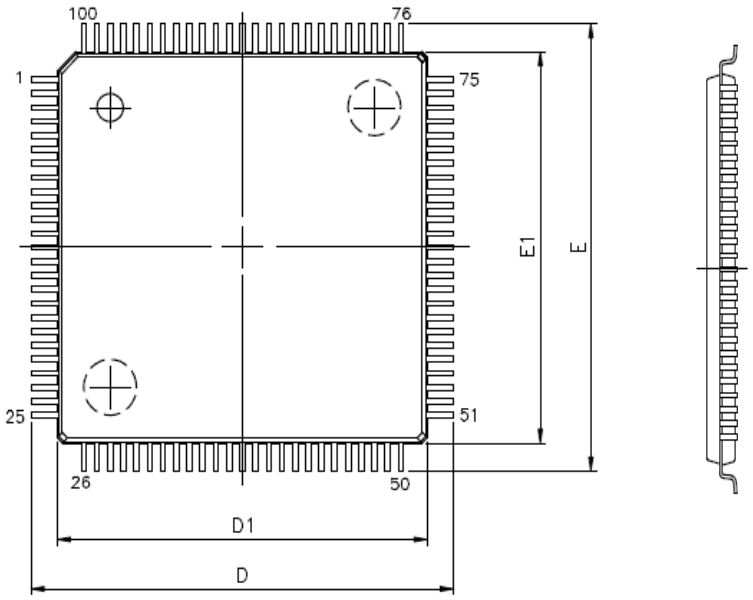
Figure 7-2 FT90XQ Top side

Notes:

1. FT90XQ symbol stands for FT900Q, FT901Q, FT902Q and FT903Q.
2. YYWW = Date Code, where YY is year and WW is week number and following character B indicates the silicon revision B.
3. Marking alignment should be centre justified.
4. Laser marking should be used.

All marking dimensions should be marked proportionally. Marking font should be using standard font (Roman Simplex).

7.3 LQFP-100 Package Dimensions



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.20	0.27
c	0.09	0.127	0.20
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		

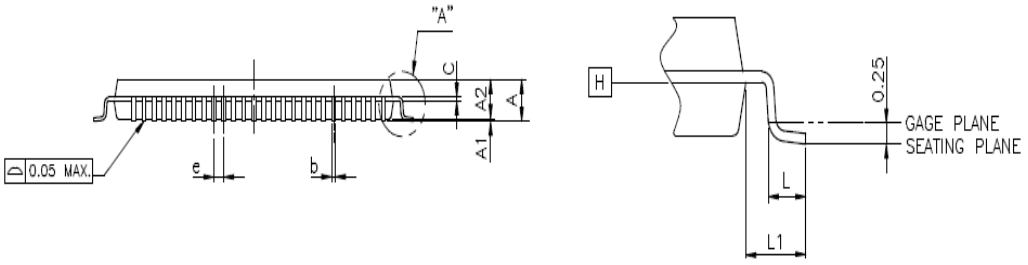


Figure 7-3 LQFP-100 Package Dimensions

7.4 LQFP-100 Device Marking

7.4.1 FT90XL Top Side

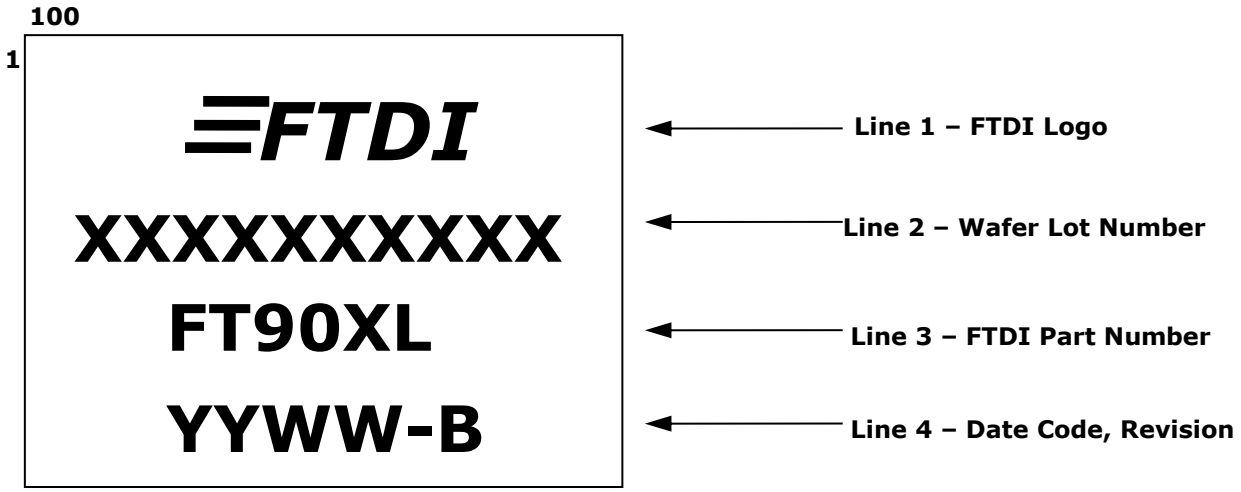


Figure 7-4 FT90XL Top side

Notes:

1. FT90XL symbol stands for FT900L, FT901L, FT902L and FT903L.
2. YYWW = Date Code, where YY is year and WW is week number and following character B indicates the silicon revision B.
3. Marking alignment should be centre justified.
4. Laser marking should be used.
5. All marking dimensions should be marked proportionally. Marking font should be using standard font (Roman Simplex).

7.5 Solder Reflow Profile

The FT90x series is supplied in Pb free QFN-100 and LQFP-100 packages. The recommended solder reflow profile for all packages options is shown in Figure 7-5.

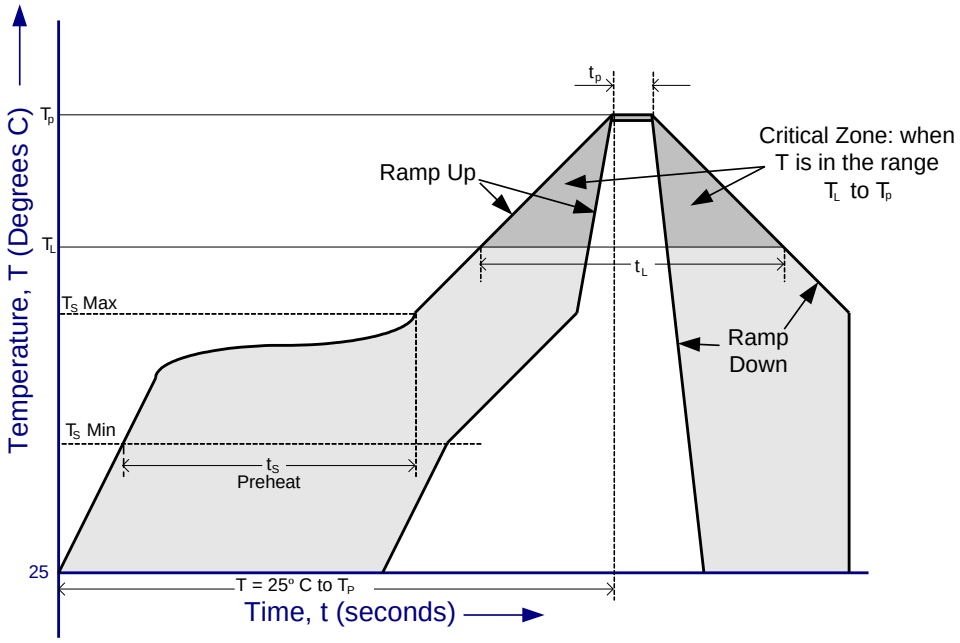


Figure 7-5 FT900 Solder Reflow Profile

The recommended values for the solder reflow profile are detailed in

Table 7-1 . Values are shown for both a completely Pb free solder process (i.e. the FT900 is used with Pb free solder), and for a non-Pb free solder process (i.e. the FT900 is used with non-Pb free solder).

Profile Feature	Pb Free Solder Process	Non-Pb Free Solder Process
Average Ramp Up Rate (T_s to T_p)	3°C / second Max.	3°C / Second Max.
Preheat - Temperature Min (T_s Min.) - Temperature Max (T_s Max.) - Time (t_s Min to t_s Max)	 150°C 200°C 60 to 120 seconds	 100°C 150°C 60 to 120 seconds
Time Maintained Above Critical Temperature T_L: - Temperature (T_L) - Time (t_L)	 217°C 60 to 150 seconds	 183°C 60 to 150 seconds
Peak Temperature (T_p)	260°C	240°C
Time within 5°C of actual Peak Temperature (t_p)	20 to 40 seconds	20 to 40 seconds
Ramp Down Rate	6°C / second Max.	6°C / second Max.
Time for T= 25°C to Peak Temperature, T_p	8 minutes Max.	6 minutes Max.

Table 7-1 Reflow Profile Parameter Values

8 Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
BCD	Battery Charge Device
CAN	Controller Area Network
CDP	Charging Downstream Port
CPI	Camera Parallel Interface
DAC	Digital-to-Analog Converter
DAQ	Data Acquisition
DCP	Dedicated Charging Port
DNL	Differential Nonlinearity
FCS	Ethernet Frame Check Sequence
FIFO	First In First Out
GPIO	General Purpose Input / Output
INL	Integral Nonlinearity
I/O	Input / Output
LQFP	Low profile Quad Flat Package
LSB	Least Significant Bit
MMC	Multimedia Card
MSPS	Mega Samples Per Second
NMI	Non-Maskable Interrupt input
POR	Power On Reset
PWM	Pulse Width Modulator
QFN	Quad Flat No-Lead

RTC	Real Time Clock
SD	Secure Digital
SDIO	Secure Digital Input Output
SDP	Standard Downstream Port
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
UHS	Ultra High Speed
USB	Universal Serial Bus

Table 8-1 Abbreviations

9 FTDI Chip Contact Information

Head Office – Glasgow, UK

Unit 1, 2 Seaward Place, Centurion Business Park
Glasgow G41 1HH
United Kingdom
Tel: +44 (0) 141 429 2777
Fax: +44 (0) 141 429 2758

E-mail (Sales) sales1@ftdichip.com
E-mail (Support) support1@ftdichip.com
E-mail (General Enquiries) admin1@ftdichip.com

Branch Office – Taipei, Taiwan

2F, No. 516, Sec. 1, NeiHu Road
Taipei 114
Taiwan, R.O.C.
Tel: +886 (0) 2 8797 1330
Fax: +886 (0) 2 8751 9737

E-mail (Sales) tw.sales1@ftdichip.com
E-mail (Support) tw.support1@ftdichip.com
E-mail (General Enquiries) tw.admin1@ftdichip.com

Branch Office – Tigard, Oregon, USA

7130 SW Fir Loop
Tigard, OR 97223
USA
Tel: +1 (503) 547 0988
Fax: +1 (503) 547 0987

E-Mail (Sales) us.sales@ftdichip.com
E-Mail (Support) us.support@ftdichip.com
E-Mail (General Enquiries) us.admin@ftdichip.com

Branch Office – Shanghai, China

Room 1103, No. 666 West Huaihai Road,
Changning District
Shanghai, 200052
China
Tel: +86 21 62351596
Fax: +86 21 62351595

E-mail (Sales) cn.sales@ftdichip.com
E-mail (Support) cn.support@ftdichip.com
E-mail (General Enquiries) cn.admin@ftdichip.com

Web Site

http://ftdichip.com

Appendix A – References

Useful Application Notes

AN_324 FT900 User Manual

AN_341 FT32 Technical Manual

Appendix B - List of Figures and Tables

List of Figures

Figure 2-1 FT900 Block Diagram 4
Figure 3-1 Pin Configuration FT900Q (top-down view) 8
Figure 3-2 Pin Configuration FT901Q (top-down view) 9
Figure 3-3 Pin Configuration FT902Q (top-down view) 10
Figure 3-4 Pin Configuration FT903Q (top-down view) 11
Figure 3-5 Pin Configuration FT900L (top-down view) 12
Figure 3-6 Pin Configuration FT901L (top-down view) 13
Figure 3-7 Pin Configuration FT902L (top-down view) 14
Figure 3-8 Pin Configuration FT903L (top-down view) 15
Figure 5-1 USB Rise and Fall Times for DP/DM 44
Figure 5-2 100Base-TX $T_{r/f}$ Timing 45
Figure 5-3 100Base-TX Jitter Timing 45
Figure 5-4 100Base-TX Transmission Waveform 46
Figure 5-5 Definition of I^2C Timing F/S mode 47
Figure 5-6 Definition of I^2C Timing HS mode 47
Figure 5-7 Definition of SPI Master Timing Mode 0 48
Figure 5-8 Definition of SPI Slave Timing Mode 0 49
Figure 5-9 Definition of I^2S Master Timing 50
Figure 5-10 Definition of I^2S Slave Timing 51
Figure 5-11 Definition of SD Host Timing 52
Figure 6-1 Crystal oscillator connection 53
Figure 6-2 External clock input 53
Figure 6-3 RTC 32.768 KHz oscillator connection 54
Figure 6-4 External 32.768 KHz clock input 54
Figure 6-5 GPIO I/O ports connection 55
Figure 6-6 USB2.0 ports connection 55
Figure 6-7 10/100Mbps Ethernet Interface 56
Figure 6-8 Unused Ethernet Connection (QFN) 57
Figure 6-9 Unused Ethernet Connection (LQFP) 57
Figure 6-10 Unused USB Connection (QFN) 58
Figure 6-11 Unused USB Connection (LQFP) 58
Figure 7-1 QFN-100 Package Dimensions 59
Figure 7-2 FT90XQ Top side 60
Figure 7-3 LQFP-100 Package Dimensions 61

Figure 7-4 FT90XL Top side 62
Figure 7-5 FT900 Solder Reflow Profile 63

List of Tables

Table 1-1 FT90x series Part Numbers 3
Table 3-1 FT900 pin description 23
Table 4-1 FT90x series default interrupt priority 27
Table 4-2 FT90x series I/O memory mapping 28
Table 5-1 Absolute Maximum Ratings 37
Table 5-2 Operating Voltage and Current 38
Table 5-3 Digital I/O Pin Characteristics (VCCIO3V3 = +3.3V, Standard Drive Level) 39
Table 5-4 USB I/O Pin (D_DP/D_DM, H_DP/H_DM) Characteristics 40
Table 5-5 Ethernet I/O pin (TXON/TXOP, RXIN/RXIP) characteristics 41
Table 5-6 DAC I/O pin (DAC_REFP, DAC0/1) characteristics 41
Table 5-7 ADC I/O Pin Characteristics 42
Table 5-8 EFUSE I/O Pin Characteristics 42
Table 5-9 System clock characteristics 43
Table 5-10 RTC clock characteristics 43
Table 5-11 Analog I/O pins (D_DP/D_DM, H_DP/H_DM) characteristics 44
Table 5-12 Analog I/O pins (TXON/TXOP, RXIN/RXIP) characteristics 45
Table 5-13 I2C I/O pins (I2C0_SCL/SDA, I2C1_SCL/SDA) characteristics 46
Table 5-14 SPI I/O pins (SPIM_CLK/MOSI/MISO/SS0/SS1/SS2/SS3) characteristics 48
Table 5-15 SPI I/O pins (SPIS0_CLK/MOSI/MISO/SS, SPIS1_CLK/MOSI/MISO/SS) characteristics 49
Table 5-16 I^2S Master I/O pins (I2S_LRCLK/BCLK/SDAI/SDAO) characteristics 50
Table 5-17 I^2S Slave I/O pins (I2S_LRCLK/BCLK/SDAI/SDAO) characteristics 51
Table 5-18 SD Host I/O pins (SD_CLK, SD_CMD, SD_DATA3/DATA2/DATA1/DATA0, SD_CD, SD_WP) characteristics 52
Table 7-1 Reflow Profile Parameter Values 63
Table 8-1 Abbreviations 65

Appendix C - Revision History

Document Title:	FT900/1/2/3 Embedded Microcontroller Datasheet
Document Reference No.:	FT_000965
Clearance No.:	FTDI#421
Product Page:	http://www.ftdichip.com/FTProducts.htm
Document Feedback:	DS_FT900_1_2_3

Version 1.0	Initial draft release	24 Feb 2014
Version 1.1	Full release	24 Sept 2015

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View FT902Q-T on WIN SOURCE
- Bridgetek Pte Ltd. Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management